

POCl₃ Annealing Effect on The Flat Band Voltage Instabilities for a SiC Based MOS Capacitor at High Temperature

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Abstract. The effect of post-oxidation annealing (POA) treatments on SiC based MOS capacitor characteristics have been investigated up to 623K, targeting operation in high temperature applications. In order to achieve the passivation of the SiO₂/4H-SiC interface and to reduce flat band voltage (V_{FB}) instabilities with temperature, the POA in POCl₃ ambient was used. The structures subjected to POA were comparatively analysed with the as-oxidized ones. High frequency capacitance-voltage (C-V) measurements were performed both at room and high temperatures on wafer and encapsulated samples. The C-V characteristics show an improved stability of V_{FB} with temperature for POCl₃ based POA samples: while the as-oxidized structures show a linear decrease of V_{FB} after 423 K, the POA leads to an increase of the temperature range where V_{FB} is approximately constant (up to 623 K).

Key words: SiC, MOS capacitor, POA, high temperature, high frequency.

1. Introduction

Harsh environment applications involve at least one of the following operating conditions: high temperature, high frequency, high power, corrosive environments, extreme vibration and high radiation [1]. Hydrogen gas sensors represent essential components in different industries such as glass, cement, chemical petroleum or automotive, where the technological process imposes exposure to harsh environments. Consequently, the development of reliable device technologies is necessary and represents a present concern [2]. Critical requirements have to be met: on one hand to ensure high sensitivity for hydrogen leakage monitoring, and on the other hand to operate at high temperatures [3].

Although silicon is the most used semiconductor material in microelectronics, when it comes to harsh environment applications (especially those that require operation at temperatures above 200°C), its electrical properties are strongly degraded. In this context, silicon carbide (SiC) becomes a valuable semiconductor material alternative, having good thermal stability due to its wide bandgap [4, 5]. Different SiC polytypes can be found in nature, but the most used are 3C, 4H and 6H-SiC [6], which present the following properties: the bandgap is ranging between 2.2 eV for cubic configuration (3C-SiC) and 3.3 eV for the hexagonal one (4H and 6H-SiC); the thermal conductivity is between 3 – 4.9 W/cmK [7]. In comparison with other wide bandgap semiconductors, SiC has the ability to grow good quality thermal oxide, albeit at a much lower rate than Si [8, 9].

The majority of SiC based gas sensors are field effect devices whose sensitivity and selectivity are higher to a broad range of gases. Furthermore, these devices are capable of fast response at a specific high temperature [10, 11, 12]. This category of gas sensors include: Schottky diodes, p-n junction diodes, metal oxide semiconductor (MOS) capacitors and MOSFETs. The detection mechanism is based on changing the interfacial polarization and transport caused by adsorption of the molecules of interest at metal-oxide interface. Consequently, the gas sensitivity is determined by the dipole layer formed at the metal-oxide interface which modifies the work function of the metal. The sensor response is influenced by several factors, including catalytic metal, oxide type, detected gas and operation temperature [13].

Regarding harsh environment applications, the hydrogen sensor based on SiC must operate properly at a temperature of at least 150°C. In this case, the response of the sensor should be hastened by the fixation of water molecules on the metal surface [14]. Table 1 reviews the main fabrication technologies proposed for SiC-based gas sensors, evidencing the electrode metals and dielectric layers used, as well as the additional fabrication processes, such as post-oxidation treatments.

The metal electrode acts as catalyst for the gas molecules' adsorption and the fulfillment of this role represents an important argument in selection of both metal type and deposition technology. It can be a continuous, very thin film, with a high surface area, but also it can be porous, thicker and stable at high temperatures. The choice of the catalytic metal depends on the type of gas which has to be detected. For hydrogen detection, metals such as Pt, Pd and Ni are most suitable [19, 20, 21]. The metal with the highest solubility of hydrogen is Pd, followed by Ni and Pt [22].

Taking into account both bandgap and thermal conductivity, the 4H-SiC polytype is generally used for high temperature hydrogen sensors. In the case of a dense and continuous metallic film, when the SiC based MOS capacitor is exposed to hydrogen, the gas molecules will dissociate on the metal surface. While a part of these molecules is adsorbed on the metal surface, some of the hydrogen atoms diffuse through the catalytic metal, arriving at the metal-insulator interface. These hydrogen atoms are polarized, forming a bipolar layer which decreases the metal-insulator work function, resulting in a left shift of the flat band voltage [23]. Contrary, when the catalytic metal is porous, the gas molecules can interact both with metal and insulator, the triple phase boundaries being required in detection of molecules. Thus, the response is determined by the presence of reaction sites, where metal surface, metal-dielectric interface and exposed dielectric surface meet [24].

The insulator selection also represents an important factor when a SiC based MOS hydrogen sensor is fabricated. It separates the metal electrode from SiC, a minimum thickness of a few nanometers being required to ensure no current flows through. Besides SiO₂, which is commonly used due to its ease of growth on SiC, different material oxides have also been studied to be used in MOS capacitors. For example, S. Kim et al. [25] have investigated SiC-based hydrogen gas sensors with MOS structures using a thin tantalum oxide (Ta₂O₅) layer for leak detection applications, providing good stability at high temperature and high permeability for hydrogen gas. Also, HfO₂ high-k dielectrics have been studied in order to obtain MOS capacitors with high electrical performances, including a thin grown SiO₂ interfacial layer [26].

In order to reduce the intrinsic mobile ions from as-oxidized SiC-MOS structures, post oxidation treatments have been reported by A. Chanthaphan et al. [27]. Different passivation techniques, such as high temperature post-oxidation annealing (POA) in an inert gas, and nitrogen-hydrogen mixed plasma exposure, have been proposed to diminish the residual carbon impurities and other defects in SiC MOS structure [28, 29]. If post-oxidation nitration processes were some of the first approaches to reduce the SiO₂/4H-SiC interface states [30], recently, phosphorous based annealing processes, both POCl₃ and PSG POA techniques [31, 32] were proposed as valuable alternatives [33].

In this paper, we analyze the Pd/SiO₂/4H-SiC MOS structure and the effect of POCl₃ annealing on its electrical properties, targeting operation in hydrogen gas sensing applications.

2. Experimental

SiC-MOS capacitor structures have been fabricated on as-grown n-type 4H-SiC epitaxial layer, having a thickness of 8 μm and doping $N_D = 2.07 \cdot 10^{16} \text{cm}^{-3}$. After the SiC substrates have been cleaned in both piranha (H₂SO₄ + H₂O₂) and 10% HF solution for 30 seconds at room temperature, a SiO₂ layer was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) from tetraethoxysilane (TEOS) at 750°C with a thickness of 1 μm. Circular windows have been opened in the passivation oxide in order to obtain the active areas of the MOS capacitor. Different

diameters, $D = 18, 24, 36,$ and $68 \mu\text{m}$, respectively, have been designed in order to obtain a MOS sensor array. An oxide ramp configuration has been achieved after an anisotropic etching, using a solution based on $\text{NH}_4\text{F}/\text{CH}_3\text{-COOH}$ (2:1). This leads to a diminishing of the negative effect of electric field crowding at the electrode corner and improves metallization conformity [34].

Table 1. Comparison of fabrication characteristics and operating parameters of previous reported SiC-based gas sensors

MOS structure	Dielectric layer	Post-oxidation annealing (POA)	Operating temp.	Gases sensed
Pt/SiO ₂ /6H-SiC [19]	SiO ₂ (43 nm) obtained in wet O ₂ at 1150°C	Ar annealing at 950°C	800 K	10% H ₂ in N ₂ , 1% O ₂ in N ₂
Al/SiO ₂ /4H-SiC [27]	SiO ₂ (40 nm) obtained in dry O ₂ for 12 h at 1100°C	– Ar annealing at 1100°C for 1 h – forming gas annealing (3% H ₂ diluted in N ₂) – 800°C for 30 min. + 450°C for 30 min.	473 K	–
Au/SiO ₂ /4H-SiC [15]	SiO ₂ (13–20 nm) obtained: in dry O ₂ at 1300°C ; in 10% of N ₂ O diluted in N ₂ at 1300°C ; in pure NO at 1175°C	–	470 K	–
Pt(100 nm)/TaSi _x (20 nm)/SiO ₂ (20 nm)/4H-SiC [16]	SiO ₂ (20nm) grown by dry oxidation	Annealing in 50% N ₂ O/Ar atmosphere	473 K	1ppm hydrogen, 2 ppm CO, 100 ppm ethane 20 ppm ethane
Pt/WO ₃ /6H-SiC [17]	WO ₃ obtained after the oxidation of a tungsten thin film (100nm) in an oxidizing atmosphere with 50% argon and 50% oxygen	–	800 K	0.125–1% hydrogen and propene in ambient
Pd(160 nm)/Ta ₂ O ₅ (120 nm)/SiC [18]	Ta ₂ O ₅ obtained by oxidation of Ta thin film in atmosphere containing oxygen	–	573 K	1000 ppm of H ₂

Figure 1 depicts the oxide ramp configuration of the four MOS structures' active areas, with a short overetching, resulting in diameters $2\mu\text{m}$ larger than designed.

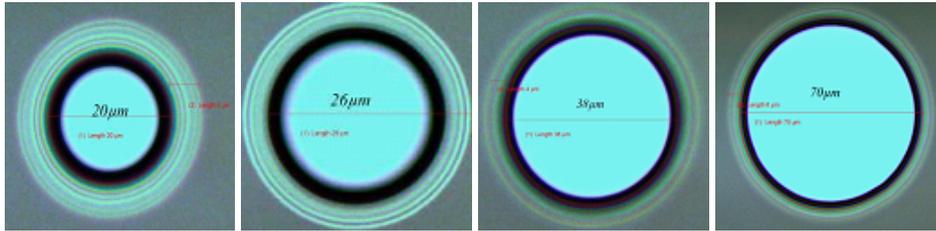


Fig. 1. Oxide ramp configuration – 4 different active areas.

Thermal oxidation has been performed at 1100°C for 3 h in dry-O₂ ambient to produce a 24 nm thick thermal oxide. The accurate profile of the ramp oxide termination was analyzed using atomic force microscopy (AFM), and in Fig. 2 both the 3D image and the profile plot of the experimental structures of SiC based MOS capacitor active area are presented.

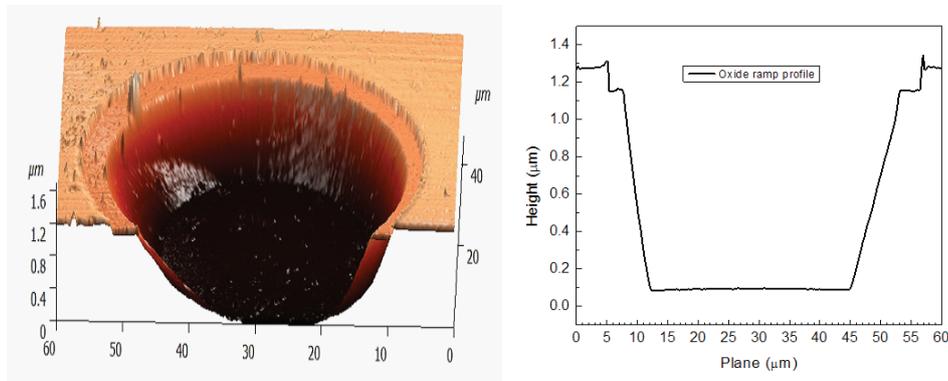


Fig. 2. Oxide ramp profile evinced by AFM analysis: a) 3D image; b) profile.

Post-oxidation annealing (POA) was conducted at 1000°C for 30 minutes in a POCl₃ ambient which was then immediately switched to N₂ for another 20 minutes. The effect of such a POA is that both phosphorous and nitrogen can passivate carbon clusters from the SiO₂/SiC interface [35]. It has been shown that a nitric oxide post-oxidation annealing and a phosphorous passivation process lead to higher inversion layer mobility, which can result in a decrease of SiO₂/4H-SiC interface trap density [32].

The gate electrode has been obtained by a sputtering deposition of a Pd thin film with a thickness of 50 nm. Subsequently, a metallic sandwich composed of Ti (15 nm) / Au (100 nm) has been deposited on both sides in order to obtain the pads and ohmic contact, respectively. In order to evaluate the parasitic capacitance, the same pads have been designed close to the active structures [36].

For packaging purposes, as shown in Fig. 3, the electrode gate of the final structure was connected to the anode terminal of a DIL16 capsule using a wire bonding technology. The chip backside is bonded using a silver paste for high temperature.



Fig. 3. Test structure bonding [36].

The MOS test structures have been electrically characterized on both wafer and encapsulated samples. Capacitance-voltage (C-V) measurements have been performed, at high frequency (1MHz) and different temperatures, using a Keithley 4200SCS.

3. Results. Discussion

3.1. Room temperature analysis

In order to determine the oxide thickness, doping and flat band voltage, high frequency C-V measurements have been carried out on wafer, at room temperature. These measurements have been done in darkness conditions, in a Faraday cage, without any outside carrier generation source. Figure 3 evinces the active capacitance variation from accumulation to the deep depletion region. The active capacitance represents the effective value of the measured capacitance subtracting the pad capacitance:

$$C_{active} = C_{measured} - C_{pad}. \tag{1}$$

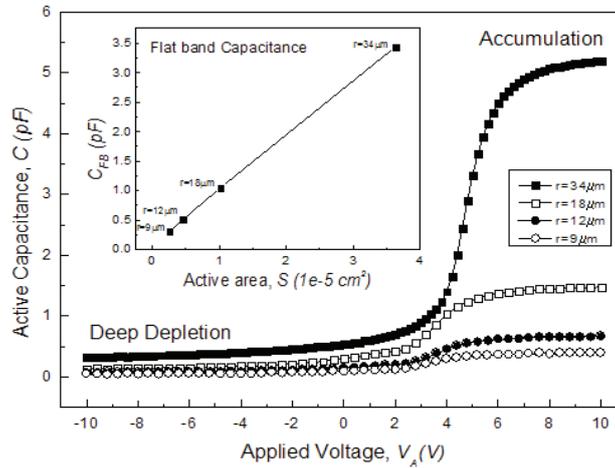


Fig. 4. C-V curves measured on wafer at room temperature.

From these measurements (Fig. 4), we can calculate the oxide thickness starting from the **accumulation** region, where the MOS capacitor is just a simple capacitor having oxide capacitance, C_{ox} . The oxide thickness extracted from these determinations is about 24 nm, for 3 h oxidation in dry-oxygen ambient. As we can see in the inset from Fig. 3, the flat band capacitance (C_{FB}) has a rising tendency with active area, according to eq. (2):

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_0 \varepsilon_{SiC} S}}, \quad (2)$$

where C_{ox} , L_D , ε_0 , ε_{SiC} and S are oxide capacitance, Debye length, permittivity of free space, SiC relative permittivity and active area, respectively. L_D can be expressed as:

$$L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{SiC} kT}{q^2 N_D}}, \quad (3)$$

where $kT = 4.046 \times 10^{-21}$ J is the thermal energy at room temperature.

When the MOS capacitor is biased in the depletion region, it behaves as two capacitors in series: C_{ox} and capacitance due to the depletion region width, C_{dep} [37]:

$$\frac{1}{C_{measured}} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}. \quad (4)$$

Moreover, the donor carrier concentration (N_D) in the SiC epi-layer was determined to be $(1.46 \pm 0.5) \times 10^{16} \text{ cm}^{-3}$ via $1/C^2$ analysis. This is consistent with the nominal donor doping density of $2.07 \times 10^{16} \text{ cm}^{-3}$. Another parameter of the MOS capacitor which can be determined from C-V measurements is the flat band voltage. There are two methods to determine this parameter:

- (a) One way is to use the flat band capacitance method. In this method, the ideal value of C_{FB} is calculated using eqs. (2) and (3). Once the value of C_{FB} is known, the value of V_{FB} can be obtained from C-V data, by interpolating the closest gate voltage (V_A) values.
- (b) Another method to calculate V_{FB} is from the Schottky-Mott model, plotting $1/C^2$ versus V_A . A straight line is obtained in a large potential interval from which flat band voltage and donor doping density are determined.

$$\frac{1}{C_{measured}^2} - \frac{1}{C_{ox}^2} = \frac{2}{q \varepsilon_0 \varepsilon_{SiC} S^2 N_D} \left(V_A - V_{FB} - \frac{kT}{q} \right). \quad (5)$$

Theoretically, V_{FB} depends on the metal work function, electron affinity of the semiconductor and can be seriously affected by the SiO_2/SiC interface states created during the oxidation process. These interface states can be residual or carbon atom clusters obtained after breaking the Si-C bonds [38].

$$V_{FB} = \psi_G - \chi_S - \frac{kT}{q} \cdot \ln \frac{N_c}{N_D} - \frac{Q_{ox}}{C_{ox}}$$

When oxide charges (Q_{ox}) are not present at the SiO₂/SiC interface (ideal case), V_{FB} practically depends only on the metal work function (ψ_G) and electron affinity of SiC (χ). Assuming that oxide charges are located at the SiO₂/SiC interface, an electric field ($-Q_{ox}/C_{ox}$) is induced in the oxide which can affect flatband voltage value, producing a shift in C–V characteristics.

3.2. Temperature analysis

Figure 4 shows high frequency (1 MHz) C–V characteristics of a 68 μm diameter *n*-type MOS capacitor in darkness, at various temperatures in the range of 298–623 K, normalized with respect to C_{ox} at 298 K.

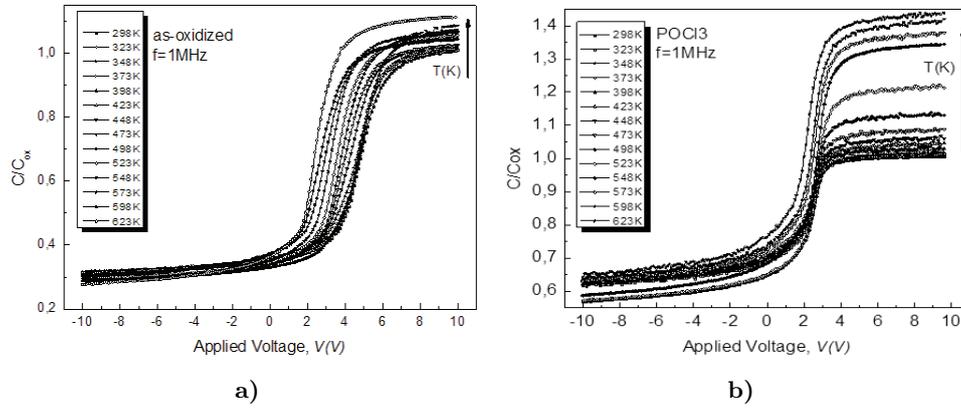


Fig. 5. High frequency C–V curves of SiC based MOS capacitor at different temperature: (a) without POA; (b) with POA.

For both samples, all the C–V curves show a negative shift when the temperature is increased. The shifts of the annealed sample are smaller than of as-oxidized one. This phenomenon could be explained by the movement of the Fermi level with temperature [39]. Another common feature to all C–V curves is that C_{ox} is increasing with temperature for each gate voltage from accumulation region. One reason could be the increase of the bulk resistance. Moreover, for the annealed sample, this fact is more pronounced due to the P atoms which increase the concentration of *n*-type dopants in the SiC interface region [32].

The flat band voltage values have been determined for both as-oxidized and POCl₃ samples via the two aforementioned methods: $1/C^2$ Schottky-Mott and flat band capacitance. The main difference between the two methods is that the C_{FB} method is more accurate when the interface states density for the SiO₂/SiC interface has low values (under 10^{12} cm⁻²).

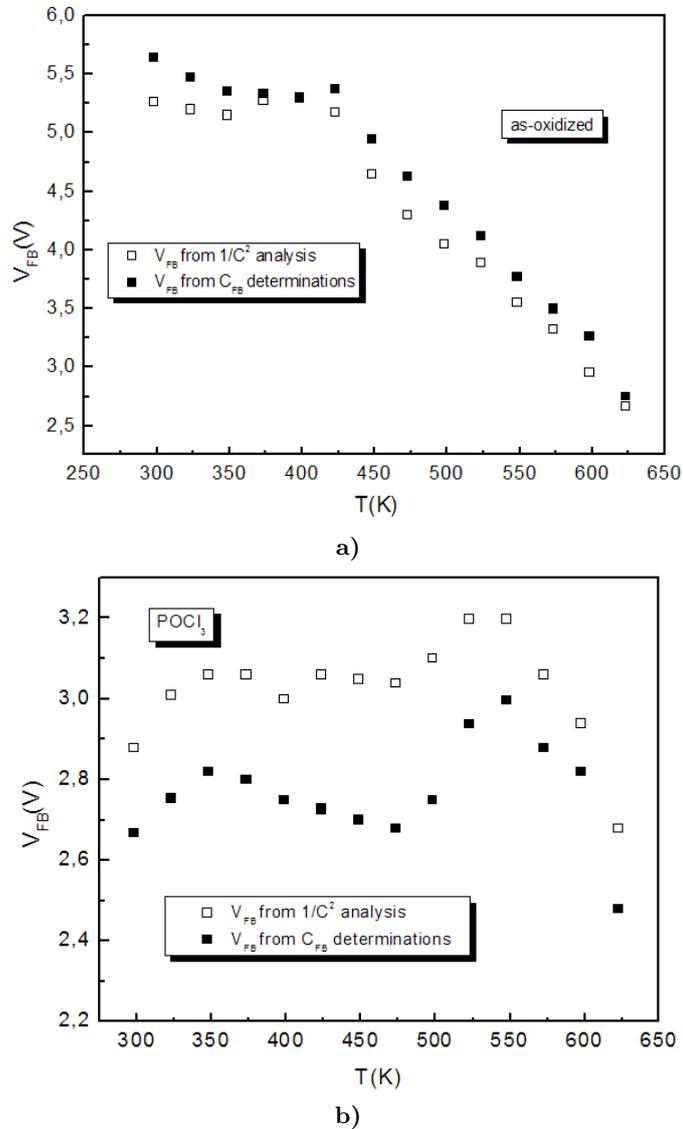


Fig. 6. The behavior of the flat band voltage with temperature for both methods on: a) as-oxidized samples; b) POCl₃ annealed samples.

For the as-oxidized sample, V_{FB} has a constant value with temperature until $T = 423$ K, after which it shows a linear decrease up to 623 K.

In contrast, the sample which suffered a POA in POCl₃ ambient has a more stable value for V_{FB} with temperature, which makes a more suitable device for gas sensing. Slight temperature shifts are considerably less likely to be mistaken for gas concentration variations, especially at higher temperatures.

4. Conclusions

The temperature behaviors of two kinds of SiC based MOS capacitors, as-oxidized and post-oxidation annealed in POCl₃ ambient have been investigated. An oxide ramp profile is achieved in order to diminish the negative effect of electric field crowding at the electrode corner and to improve the metallization conformity.

Room temperature analysis led to the determination of oxide thickness and doping concentration. The flat band capacitance had an increasing linear variation with the active area of the MOS capacitor.

A proper stability at high temperature was exhibited by both samples. All the C-V curves showed a negative shift when the temperature was increased due to the movement of the Fermi level with temperature. The post-oxidation annealed sample showed a better temperature behavior (smaller shift) due to the passivation effectiveness of the treatment. Oxide capacitance variation with temperature was also more pronounced for the annealed sample due to the P atoms which increase the concentration of *n*-type dopants in the SiC interface region.

The flat band voltage was evaluated for both samples using two methods. The temperature dependence of V_{FB} exhibited a better stability for the annealed sample, showing minor variations for the entire temperature range. By comparison, the as-oxidized device presented a linear decrease in V_{FB} after 423 K.

The overall superior temperature stability of the treated sample have determined that devices subjected to a post-oxidation annealing process in POCl₃ are recommended, in favor of their as-oxidized counterparts, for use as gas sensors in harsh environment applications.

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