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Burst Mode Switched Capacitor Voltage Converter Modeling and Design

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Abstract. An inductorless switched - capacitor (SC) DC-DC voltage converter and a model based on the averaging technique are presented. The model was validated through circuit level simulations for a SC converter designed using CMOS 0.18 um technology, capable to deliver output currents up to 100 mA at a regulated low ripple 3.3 V output voltage, for input voltages between 1.8 V and 3.2 V and can be used for other design specifications as well. The converter automatically switches to burst mode when the output current decreases. The value of the output current is detected without the use of inductors or resistors.

Key words: switched capacitor DC-DC converter, average small signal model, dynamic behavior, stability, burst mode.

1. Introduction

SC voltage converters represent the best choice of voltage regulation from the efficiency and area consumption point of view. One method to regulate a voltage by means of switched capacitors is to use a variable operating frequency depending on the output load. This kind of solution, one being reported in [1] has the disadvantage of variable output ripple, i.e., high output noise. In [2], a pseudo-continuous control is employed to control the amount of charge transferred from the input voltage to the output, and was shown to exhibit high efficiency and good transient response, even in the case of rapid load variation. However, using variable switching frequency, the output noise spectrum is large.

In [3], a sigma – delta control loop was used to reduce the tones present in the output noise. By using fixed frequency, very low output ripple can be obtained. Solutions using fixed frequency have been reported in [4–7] as well.

In [8] a dynamic model for a double and triple charge pump is presented. The model takes into account parasitic capacitances and leakage currents. In [9], a study of the theoretical performances of SC voltage multiplier circuits is reported, and the complete set of attainable DC conversion ratios is determined. The dynamics of the Dickson charge pump are analyzed in [10], the results allowing for an estimation of the rise time and power consumption during boosting. In [11], the power stage of the regulator is simulated by means of step wise integration through a progressive analysis of the states of the switches.

However, fixed frequency converters have the disadvantage of rapid efficiency decrease with the decreasing of the output current. To prevent efficiency decrease, the voltage converter can be design to work in "burst mode". Burst mode solutions are presented in [5–8]. While in [5] and [6] the solutions for detecting the value of the output current are based on the use of inductors, in [7], a step/down only solution is presented.

In this paper we present a SC DC-DC voltage converter, a model based on averaging techniques and a mechanism for automatically switching to one of the two modes, of operation normal or burst which uses neither inductors nor resistors as sensors for detecting the value of the output current.

2. Switched capacitor DC-DC voltage converter

The core schematic of a switched-capacitor DC-DC voltage converter is presented in Fig. 1. The circuit "converts" the input voltage, V_{in}, into a regulated output voltage, V_{out}, by means of a capacitor C_F which is charged from the input in the first phase, and partially discharged on the load in the second phase. The level of the output voltage is set by the reference voltage (V_{ref}). The use of NMOS transistors for (S_1, S_2) and PMOS transistors for (S_3, S_4) requires the clocks to be "one on top of the other", as illustrated in Fig. 3.

To maintain a fixed output voltage, a feedback loop is used to control the amount of charge transferred from the input to the output. The loop consists of a resistive divider ($R_1 + R_2, R_3$), an error amplifier, a voltage reference and a current mirror and works as follows: as long as the down scaled version of the output voltage connected at the noninverting input of the error amplifier is less then V_{ref}, the output of the amplifier is low and the gate to source voltage of Q_1 is large. These results in a low ON resistance for transistor Q_1, and a maximum charge can be transferred from the input to the output. The value of this maximum charge depends on the charge pump operating frequency, the flying capacitor, the equivalent series resistance of capacitors C_F, C_L, the minimum ON resistance of switches, minimum ON resistance of transistor Q_1, and the "dead time" of the pump – the time in which none of the two pairs of switches are ON. As soon as the output voltage level is reached, the output of the error amplifier begins to increase. This increases the ON resistance of Q_1, which, in turn, limits the amount of charge been transferred to the output.

Depending on the input voltage, the reference and the output load, the error amplifier output will eventually reach a value such that only the charge necessary to

maintain a steady output is transferred.

Charge transfer limitation is employed on both phases of operation, the equivalent circuits corresponding to each phase of operation being presented in Fig. 2. This solution allows a designer to easily modify the converter for using two flying capacitors, to further reduce the output voltage ripple, and has the drawback of increasing the open loop resistance, reducing thus the efficiency of the converter.

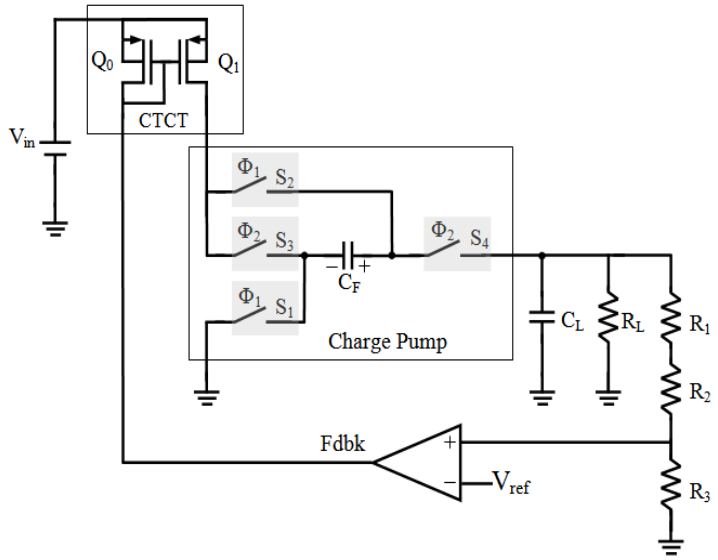

Fig. 1. Schematic of the SC DC-DC voltage converter, (S_1, S_2) are NMOS and (S_3, S_4) – PMOS transistors. C_F and C_L are external "fly" and "storage" capacitors respectively.

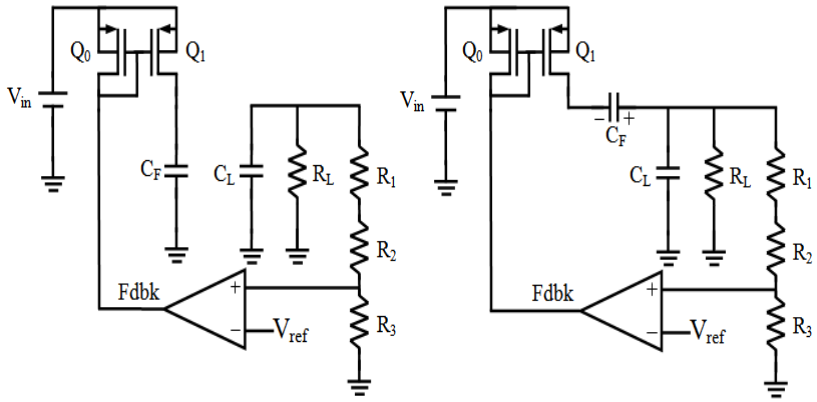

Fig. 2. Equivalent circuits corresponding to each phase of operation: charging C_F from the input voltage (V_{in}) and discharging part of the charge stored in C_F on the output load (C_L, C_L, R_L).

Several relations involving the open loop resistance, the operating frequency and the efficiency of the converter presented in Fig. 1 are given bellow.

- Power loss:
$$P_{LOSS} = I_{out}^2 R_{OL} + I_q V_{in}, \tag{1}$$
where R_{OL}, the open loop resistance, is:
$$R_{OL} \cong 4(2R_{sw} + R_V + ESRC_F) + ESRC_L + 1/f_{osc}C_F, \tag{2}$$
- $ESRC_F$, $ESRC_L$ – equivalent series resistance of capacitors C_F and C_L, respectively,
- R_{sw} – switch resistance,
- R_V – resistance of transistor Q_1,
- $I_q V_{in}$ – quiescent power dissipation,
- I_q – current absorbed by the control circuitry,
- $1/f_{osc}C_F$ – inherent switched capacitor resistance,
- Efficiency:
$$\eta = \frac{V_{in}I_{in} - R_{OL}I_{out}^2}{V_{in}I_{in}}, \tag{3}$$
- Output Ripple:
$$\Delta V_{out} \approx \frac{I_{out}}{2f_{osc}C_L} + 2I_{out}ESRC_L. \tag{4}$$

The efficiency of the converter discussed above for various input voltages and two values of the load currents, obtained at transistor level simulation, is presented in Fig. 4. The simulations have been run using $C_{in} = C_L = C_F = 2.2$ uF (C_{in} is the capacitor connected in parallel with the input voltage), and for a fixed output voltage $V_{out} = 3.3$ V.

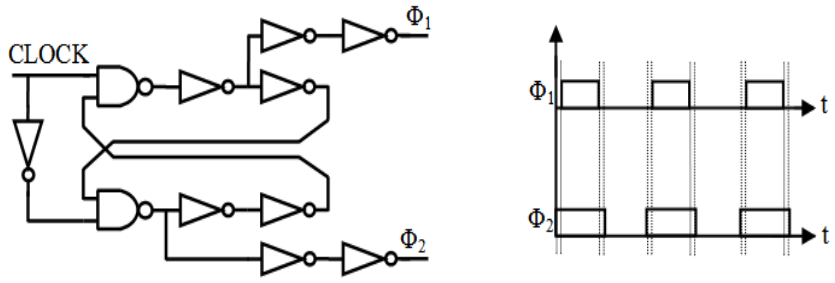

Fig. 3. Nonoverlaping signal clock generator.

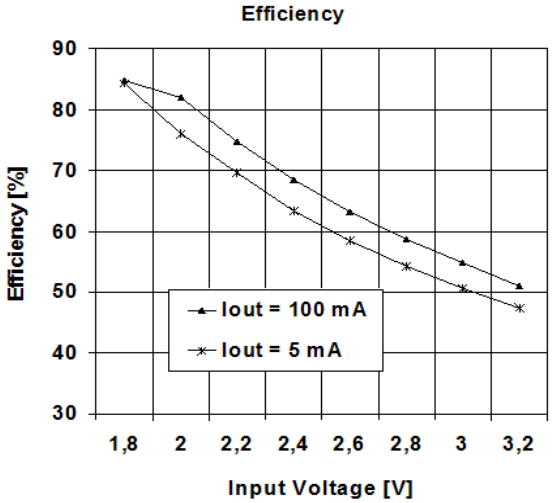

Fig. 4. Efficiency of the DC-DC voltage converter.

It can be seen that there is a significant efficiency decrease with the increase of the input voltage. It is also evident that in the case of very low output currents ($I_{out} = = 5$ mA) there is an additional efficiency drop. This further decrease is due to the switching losses that become prohibitively large for low output currents.

2.1. Converter model

In the following a small signal model developed for the SC DC-DC voltage converter discussed above will be presented.

2.1.1. Model derivation

In Fig. 5 the models used for each phase of operation are presented, where R' and R'' model the ON resistances of the switches and the resistance of Q_1 during each phase of operation, V_g is the input voltage, C_F, C_L are the "fly" and "storage" capacitors, respectively and R_L (G_L) the load resistance (conductance).

Writing the equations for each phase of the charge pump and using as constrains $< i >=< i_1 >= 0$ where $< . >$ represent mean values, the following set of equations is obtained:

$$\begin{cases} C_F \dfrac{d < V >}{dt} = G'(< V_g > - < V >) - G''(< V_g > + < V > - < V_L >), \\ C_L \dfrac{d < V_L >}{dt} = G''(< V_g > + < V > - < V_L >) - 2G_L < V_L > \end{cases}, \quad (5)$$

where all mean variables have been considered as sums of a constant and a slowly variable component:

$$< V >= V + \hat{v}, \quad < V_L >= V_L + \hat{v}_L, \quad < V_g >= V_g + \hat{v}_g, \tag{6}$$

and represent the voltages across C_F, C_L and the input voltage, respectively.

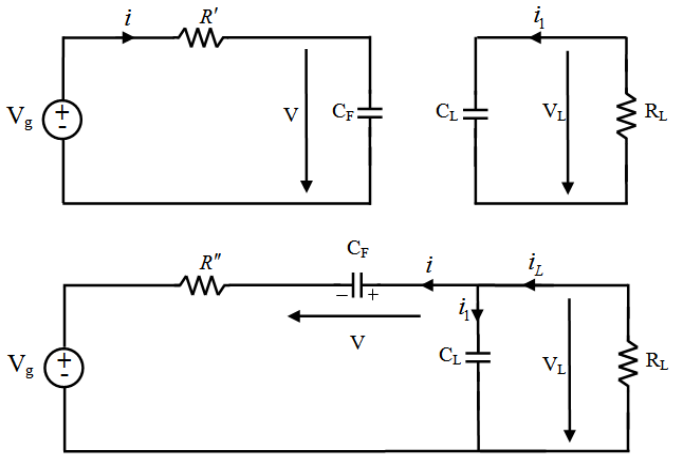

Fig. 5. SC DC-DC voltage converter model for each phase of operation.

The steady state (mean value) solution of the output voltage is:

$$< V_L >= \frac{2R_L V_g}{2R' + 2R'' + R_L}. \tag{7}$$

In order to linearly model the dependence of the conductance on control voltage, the following expressions for $G_0^{'}$ and $G_0^{''}$ are used:

$$G_0' = 1/R';\ G_0'' = 1/R'', \tag{8}$$

$$G' = G_0' + k_1 \hat{U}_c,\ G'' = G_0'' + k_2 \hat{U}_c,\ k_1, k_2 < 0, \tag{9}$$

where $\hat{U}_c$ represents the variation of the error amplifier output voltage (Fdbk), G_0' and G_0'' the conductance of each of the two pairs of switches, including that of Q_1 for the case U_c=0, for phase 1 and 2, respectively, k_1, k_2 are the slope variation of the conductance of Q_1 during each phase. The (almost linear) variation of the conductance of Q_1 with respect to U_c, for an output current value of 50 mA , input voltage of 2.3 V and for an output voltage of 3.3 V, simulated at transistor level, is presented in Fig. 6.

From Fig. 6 it is apparent that the conductance varies almost linearly with the U_c voltage.

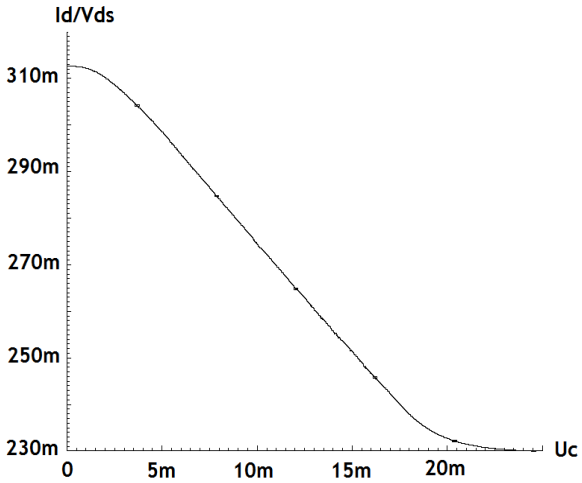

Fig. 6. Variation of the Q_1 transistor conductance as a function of U_c.

In Fig. 7, the difference between the output voltage at transistor level simulation and the output voltage computed with the proposed model with respect to the voltage reference is presented. It can be seen that, for small variations, the output error is less than 5%. Therefore, the values for k_1 and k_2 need to be updated at every 30 mV increase/decrease of the voltage reference.

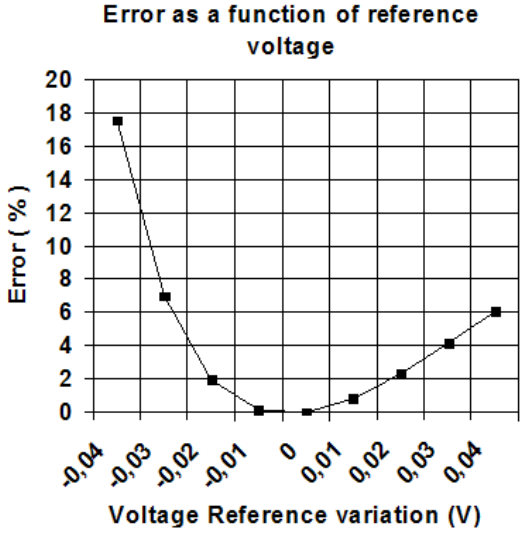

Fig. 7. Output error as a function of the voltage reference variation.

From (5) and using (6),(8) and (9) we have:

$$\begin{cases} C_F \dfrac{\mathrm{d} < \hat{v} >}{\mathrm{d}t} = (G_0' + k_1 \hat{u_c})[V_g + \hat{v_g} - (V + \hat{v})] - \\ -(G_0'' + k_2 \hat{u_c})[V_g + \hat{v_g} + V + \hat{v} - (V_L + \hat{v_L})], \\ C_L \dfrac{\mathrm{d} < \hat{v}_L >}{\mathrm{d}t} = (G_0'' + k_2 \hat{u_c})[V_g + \hat{v_g} + V + \hat{v} - (V_L + \hat{v_L})] - \\ -2G_L(V_L + \hat{v_L}). \end{cases} \tag{10}$$

Working out the equations and removing the nonlinear terms, the following system of differential equations is obtained:

$$\begin{cases} C_F \dfrac{\mathrm{d} < \hat{v} >}{\mathrm{d}t} + \hat{v} G_1 = G_0' \hat{v}_g + \hat{u}_c(k_1 N - k_2 M) - G_0'' \hat{v}_g + G_0'' \hat{v}_L, \\ C_L \dfrac{\mathrm{d} < \hat{v}_L >}{\mathrm{d}t} + \hat{v}_L G_2 = G_0'' \hat{v}_g + G_0'' \hat{v} + k_2 \hat{u}_c M, \end{cases} \tag{11}$$

where:

$$G_1 = G_0' + G_0'', \ G_2 = G_0'' + 2G_L, \tag{12}$$

$$M = V_g + V - V_L, \ N = V_L - V. \tag{13}$$

A model of the charge pump corresponding to above equations is shown in Fig. 8, where $\hat{i_L}$ is introduced tot model the variation of the output current.

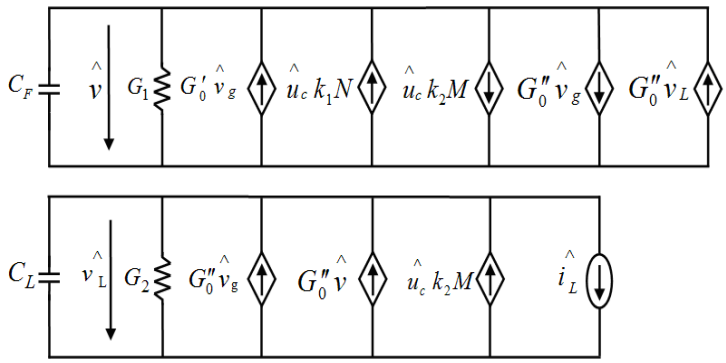

Fig. 8. SC DC-DC voltage converter model.

Using the Laplace transform, the following output voltage variation $\hat{v_L}$ is obtained:

$$\hat{v_L} = \frac{H_u(s)}{P(s)} \hat{u_c} + \frac{H_g(s)}{P(s)} \hat{v_g} + \frac{Z_L(s)}{P(s)} \hat{i_L}, \tag{14}$$

where:

$$P(s) = s^2 C_L C_F + s[C_L(G_0' + G_0'') + C_F(G_0'' + 2G_L)] + 2G_L(G_0' + G_0'') + G_0' G_0'', \quad (15)$$

$$H_g(s) = G_0''(sC_F + 2G_0'), \quad (16)$$

$$H_u(s) = [k_2 M(sC_F + G_0') + G_0'' k_1 N], \quad (17)$$

$$Z_L(s) = -(sC_F + G_1). \quad (18)$$

The block diagram of the feedback system, where $H_d(s) = R_3/(R_1 + R_2 + R_3)$ and A(s) is the transfer function of the error amplifier, is presented in Fig. 9.

The expressions of $\hat{v}_L$ with the loop open and closed are respectively:

$$\hat{v}_{L\_openloop} = \hat{v}_{ref} A(s) H_u(s) + \hat{v}_g H_g(s) + \hat{i}_L Z_L(s), \quad (19)$$

$$\hat{v}_L = \frac{\hat{v}_{ref} A(s) H_u(s) + \hat{v}_g H_g(s) + \hat{i}_L Z_L(s)}{1 + H_d(s) A(s) H_u(s)}. \quad (20)$$

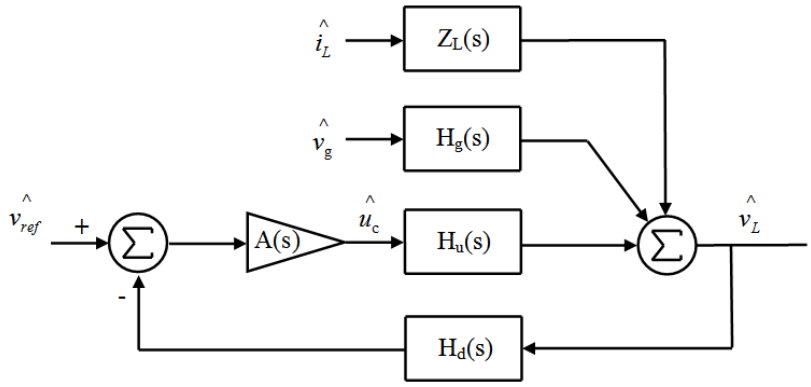

Fig. 9. Block diagram of the SC DC-DC voltage converter small signal model.

2.1.2. Model validation

The validation of the model in terms of transient and steady state response, and the stability analysis performed on the entire switched capacitor converter, is discussed below.

Stability analysis has been performed using the block diagram presented in Fig. 9 with parameters taken from the transistor level realization. The corresponding root locus is presented in Fig. 10 and shows that the voltage converter is stable for an open loop gain less than 1.67×10^6.

To further validate the model, a series of simulations have been run in Simulink and the obtained results compared with the transistor level simulation results in Cadence, a couple of results being shown in Fig. 11 and Fig. 12.

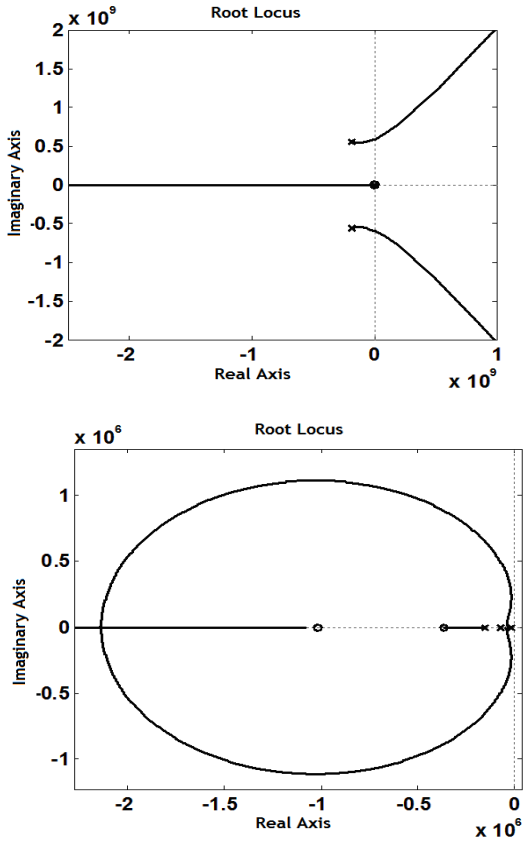

Fig. 10. Root locus diagram corresponding to the switched – capacitor DC-DC voltage converter.

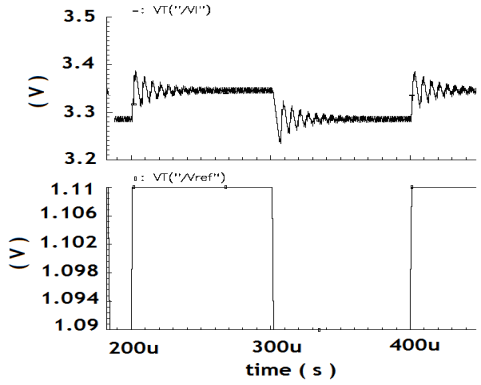

Fig. 11. Cadence simulation for the case $V_{in} = 2.34$ V, $I_{out} = 50$ mA. The reference voltage varies from 1.09 V to 1.11 V (20 mV), $t_{rise}/t_{fall} = 1$ us.

From Fig. 11 and Fig. 12 it can easily be seen that the results obtained in Simulink are very close to those obtained in Cadence. In both cases, the steady state output voltage has the same variation (60 mV) at the same voltage reference variation (20 mV in this case) while the settling time in Simulink is slightly smaller.

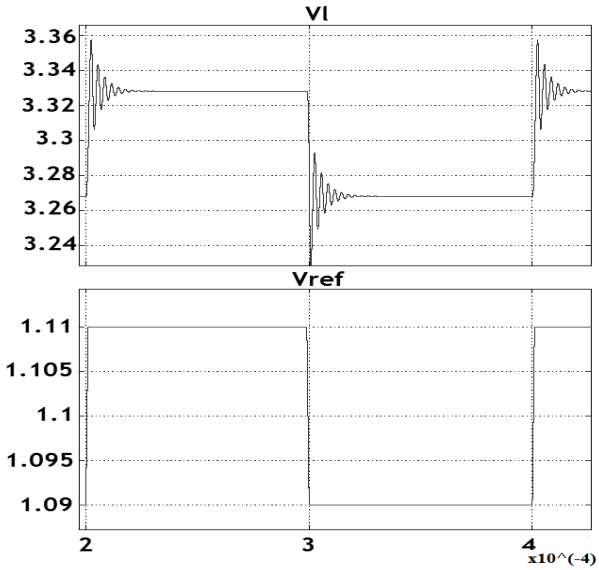

Fig. 12. Simulink results for the case of $V_{in} = 2.34$ V, $I_{out} = 50$ mA. The reference voltage varies from 1.09 V to 1.11 (20 mV), $t_{rise}/t_{fall} = 1$ us.

2.2. Burst mode

A major drawback when using fixed frequency is the significant efficiency decrease in the case of weak loads, when power losses due to switching become prohibitively large. The high switching power loss is a consequence of using large transistors with inherently large capacitances as switches. Moreover, for each switch, a chain of inverters need to be used, to ensure a minimum switching time delay.

To prevent switching power loss and therefore, efficiency decrease in the case of weak output loads, the voltage regulator can be designed to switch to *burst mode* when the oscillator is stopped and is turned on only when the output voltage decreases bellow a minimum allowable value, and new charge to compensate the loss is required. By turning the oscillator on only for short periods of time, the switching loss is reduced to a minimum possible.

The complete voltage converter schematic presented in Fig. 13, consists of the model control circuit (MCC) used to detect the value of the output current and switch to and from burst mode, the soft start and short circuit protection circuit, the charge pump, the oscillator, the reference generator, the charge transfer control and the thermal shut down block.

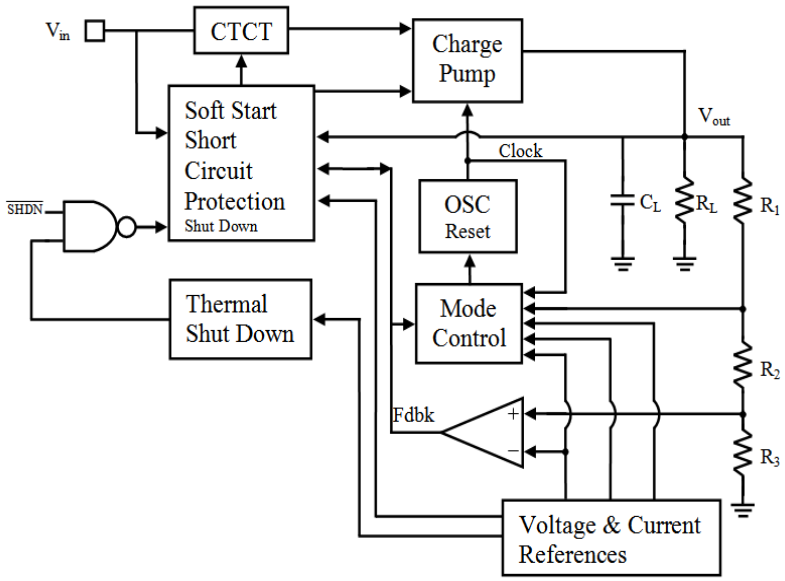

Fig. 13. Complete schematic of the switched capacitor DC-DC voltage converter.

2.2.1. Mode control circuit (MCC)

The MCC uses information from two distinct points, the output of the error amplifier (Fdbk) for entering burst mode, and the average value of the clock signal for exiting burst mode. By using charge transfer control on both charge pump phases, the output of the error amplifier reflects very well the value of the output current when working in normal mode, while in burst mode, the average number of clock pulses needed to compensate the output voltage drop are in good correspondence with the value of the output current, i.e., vary almost linearly with it.

The MCC presented in Fig. 14 is fairly simple, uses small silicon area, and none of the elements except for the transistor and the resistor connected in source follower configuration, should have small tolerances, making it less sensitive to technology variations. However, the burst mode thresholds rely on the use of a good voltage reference circuit.

The MCC works as follows: As soon as the output voltage dictated by the reference is reached, the error amplifier output (Fdbk) will settle at a value such that the charge transfer from the input to output only compensates the output current drained by the load. With the decreasing of the output current, the Fdbk is increasing to maintain the same output voltage. Fdbk voltage is in good correspondence with the output current, and so, a shifted value of the input voltage (V_{ref3}) can be used as reference for entering burst mode in order to maintain the same threshold for the entire input voltage range. For smoothing the Fdbk signal the upper RC filter is employed and the comparison between Fdbk and V_{ref3} is performed by the upper comparator (COMP).

When V_{ref3} has increased above Fdbk, the comparator will switch high and will trigger the voltage converter to work in burst mode.

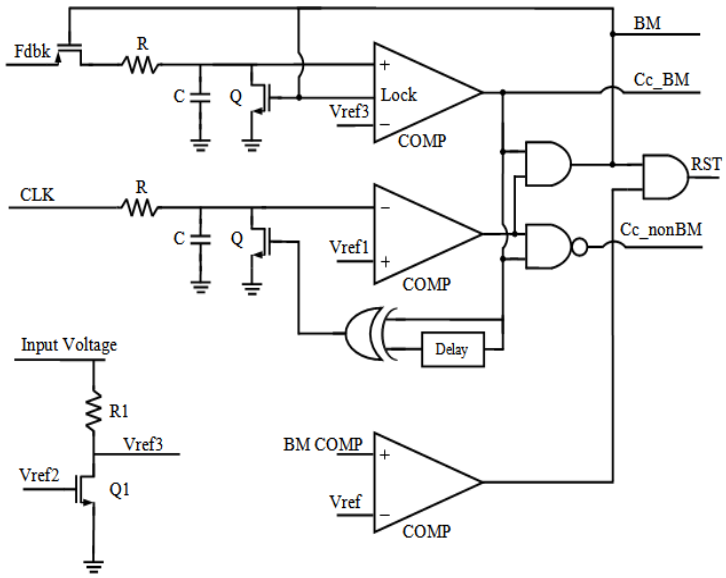

Fig. 14. Mode control circuit.

Once entered burst mode, the mean clock signal is monitored, its value being obtained at the output of the lower RC filter. Immediately after entering burst mode, the output of the filter is turned to zero for a short period of time by means of transistor Q which is turned ON.

After the upper comparator has been locked in HIGH, and the pMOS transistor turned OF, if the output voltage is higher or at least equal to the value dictated by V_{ref}, the lower comparator will also be HIGH. When both inputs of the right hand side AND logic gate are high, its output (RESET) will be HIGH and the oscillator stopped.

When the output decreases due to the load current, the lower comparator will switch LOW and will enable the oscillator. As soon as the output drop is compensated, the comparator will switch back HIGH and stop the oscillator. This cycle is repeated as long as the output current remains lower than the threshold at which the voltage regulator will switch back to the normal mode.

When the output current increases, the lower comparator must switch low more often, increasing thus the average clock. When the average clock overcomes Vref1, the middle comparator switches low and the converter works in normal mode.

The MCC works in a master – slave, slave – master configuration. When in normal mode, the upper comparator decides when to switch to burst mode, while when working in burst mode, the middle comparator decides when to switch back to normal mode (Continuous Clocking Mode – CCM).

The error amplifier monitors the output voltage in both modes of operation to ensure low output ripple. The lower comparator will monitor a divided output voltage level which is slightly higher than that monitored by the error amplifier. This ensures that the oscillator will be turned on only after Fdbk had decreased by a significant amount, to allow for a significant charge to be transferred from the input to the output, beginning with the first clock pulse.

The RC filters used in the MCC have large time constants because in the case of the upper one, a larger time constant prevents the converter for accidentally entering burst mode for large output variations when the Fdbk has a large excursion, while the lower one must smooth a signal consisting of a pulses trains.

2.2.2. Error amplifier

The error amplifier must ensure good stability and low output ripple in both modes of operation.

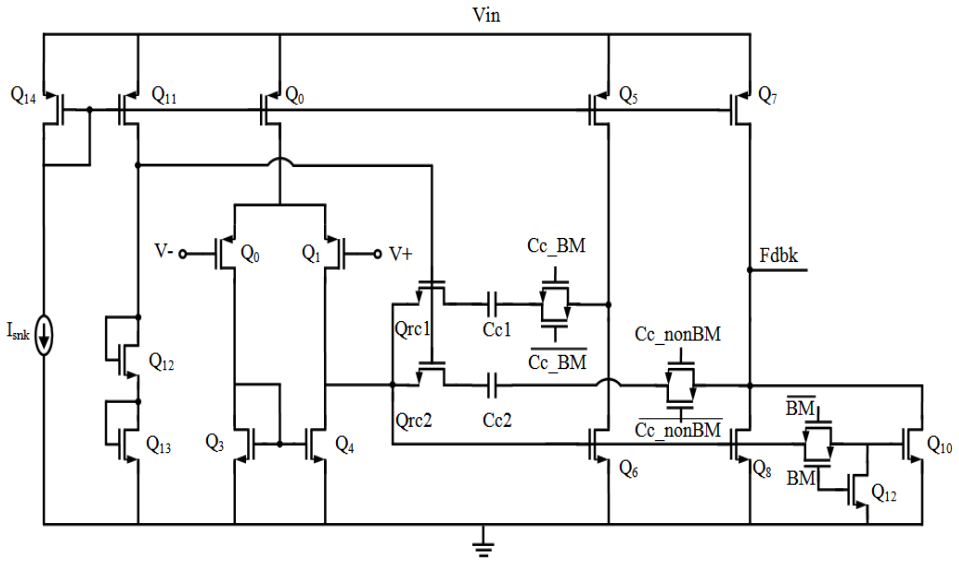

Fig. 15. Schematic of the error amplifier.

In normal mode, the amplifier must ensure minimum output voltage error and maximum possible charge transfer, to reduce the overall open loop resistance, while in burst mode, it must have a high slew rate and reduced power consumption, to increase efficiency and reduce the output ripple. In both modes of operation the amplifier should have good phase margins to ensure the overall stability of the entire converter.

The requirements for the error amplifier in the two modes of operation are accomplished by the amplifier presented in Fig. 15.

The amplifier has two output stages connected in parallel, each with its Miller compensating loop, one output stage being used to control the CTCT block, while

the second one compensates the amplifier when working in burst mode. The output stage used to control the gate to source voltage of the CTCT has a different gain for each mode of operation.

When working in normal mode the compensation of the amplifier is done by $Q_{rc2}C_{c2}$, and in burst mode by the $Q_{rc1}C_{c1}$.

The switching between the loops is done in such a way to ensure that at least one loop is active at any given moment. When switching from one mode to the other, both loops may be active for a short time interval.

2.2.3. Soft start and short circuit protection mechanism

Another important block of the converter is the soft start mechanism; its task is to prevent rush input current during initialization of the converter and to ensure protection in case of accidentally output short circuit. The mechanism is presented in Fig. 16.

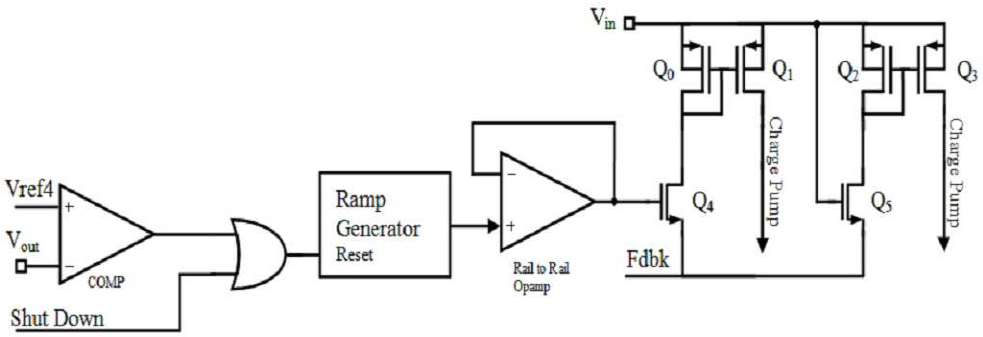

Fig. 16. Soft Start and the Short Circuit protection mechanism.

The mechanism ensures a "soft start" by slowly increasing the charge transfer. This is done as follows: when the circuit is started or is recovering from a thermal shut down, the output voltage (V_{out}) is lower than V_{ref4}, COMP is high and the ramp generator (RG) block is in reset mode. This results in the output of the rail to rail amplifier (RRA) to be zero and therefore transistor Q_4 is OFF. In this case, Q_0, Q_1 are both OFF and the current passing transistor Q_1 is extremely small. Q_0, Q_1 form the main current mirror and must be ON for maximum charge transfer. While Q_0, Q_1 are OFF, the charge transfer is ensured by Q_3. The current mirror Q_2, Q_3 allows for a minimum charge transfer, needed only to ensure that if the output is not short circuited, V_{out} will overcome V_{ref4}. When $V_{out} > V_{ref4}$, COMP will switch high and the RG output will increase linearly from zero to V_{dd}. As the RG output increases, so does the voltage at the gate of transistor Q_4 turning it ON. As Q_4 is more opened, the charge transfer increases due to higher current passing through Q_1. Eventually, depending on the time constant of the RG, the output of the RR Opamp will be equal to V_{dd} and Q_4 transistor turned ON. If by accident the output is short circuited or the temperature of the circuit increases above the designed thermal threshold, the cycle will repeat indefinitely.

3. Results

The simulations results presented bellow have been obtained using $C_{in} = C_L = C_F = 2.2$ uF (C_{in} – capacitor connected in parallel with the input voltage source), $T = 27°$C, $V_{in} = 2.34$ V (unless otherwise specified), and for fixed output, $V_{out} = 3.3$ V.

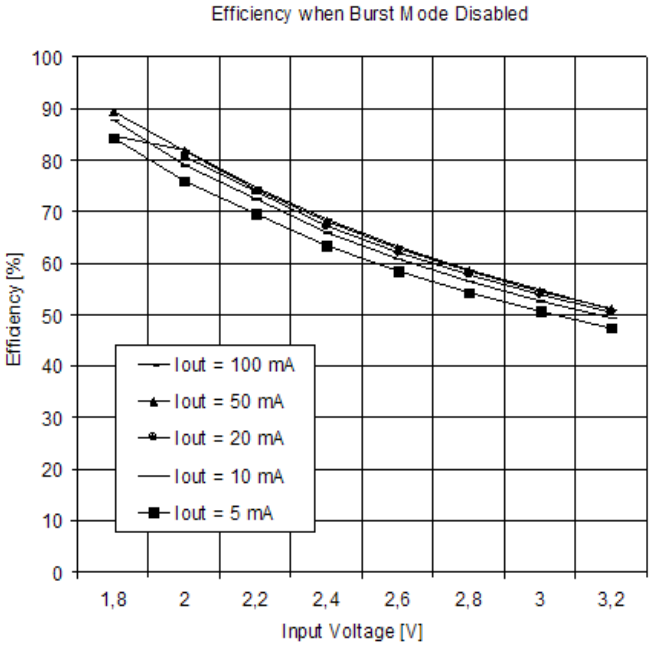

Fig. 17. Efficiency when converter is working in normal mode.

In Fig. 17 the efficiency when the converter is working in normal mode for different input voltages and output currents is presented.

The output voltage ripple when the converter is working in normal mode, for different output currents is presented in Fig. 18. It can easily be seen that the output ripple decreases as the output current decreases.

The behavior of the converter during soft start for different input voltages and for an output current $I_{out} = 100$ mA is presented in Fig. 19. Depending upon the value of the input voltage, the time interval required to reach the output voltage is different. It is evident that the output voltage overshot is very small.

The efficiency when the converter is working in burst mode is presented in Fig. 20. From Fig. 17 and Fig. 20 it is evident that in burst mode, the efficiency is higher for low output currents.

The price for an increased efficiency is paid in terms of output voltage ripple. The output voltage ripple and the clock signal when the converter is working in burst mode are presented in Fig. 21. It can be seen that the clock is ON only for short

periods of time while the output voltage ripple is still very small in comparison with the output voltage.

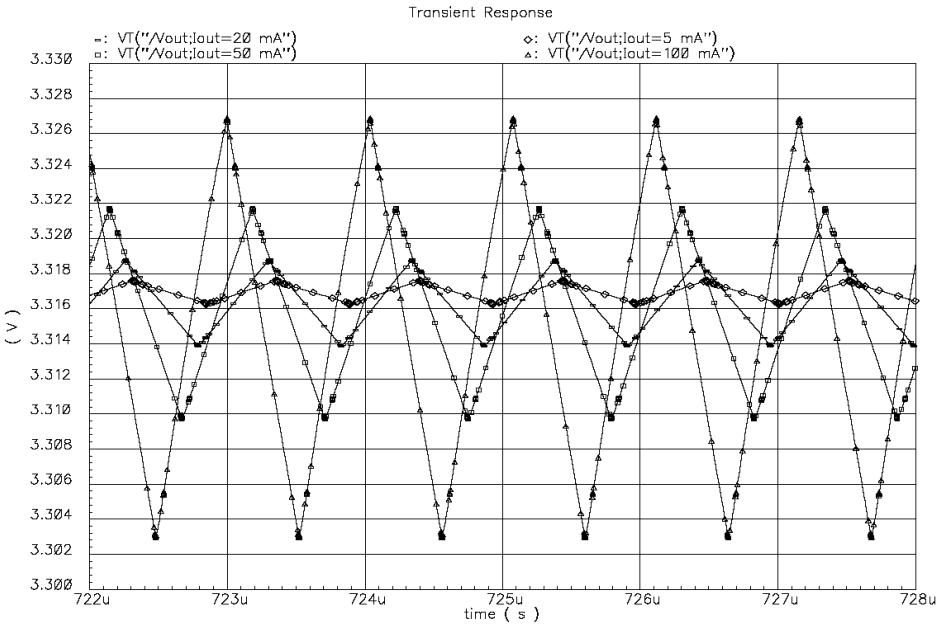

Fig. 18. Output ripple vs. output current.

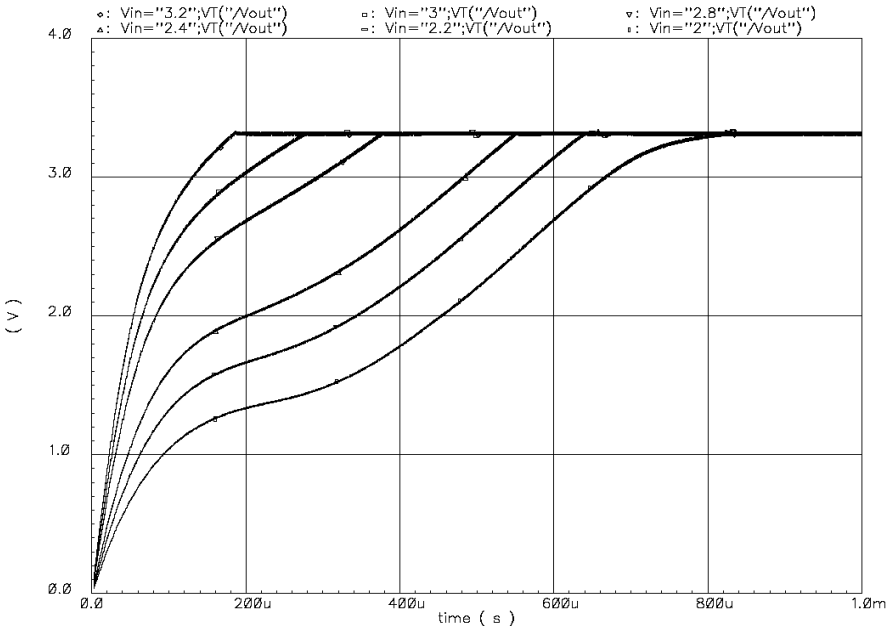

Fig. 19. V_{out} during Soft Start.

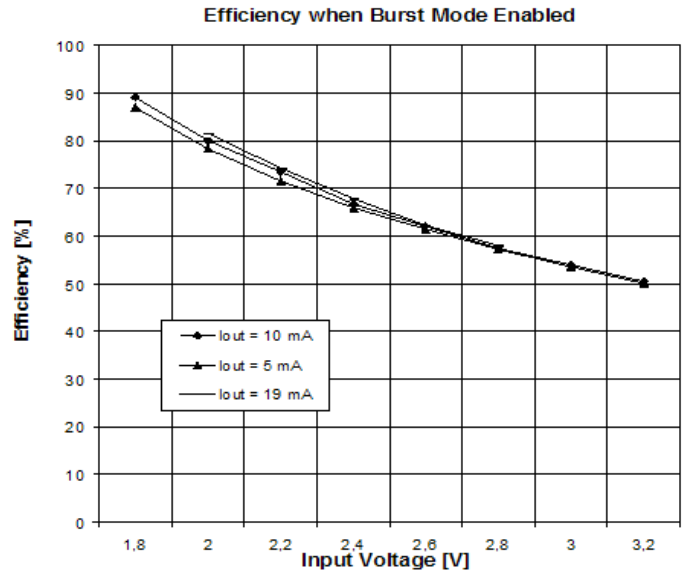

Fig. 20. Efficiency when the converter is working in Burst Mode.

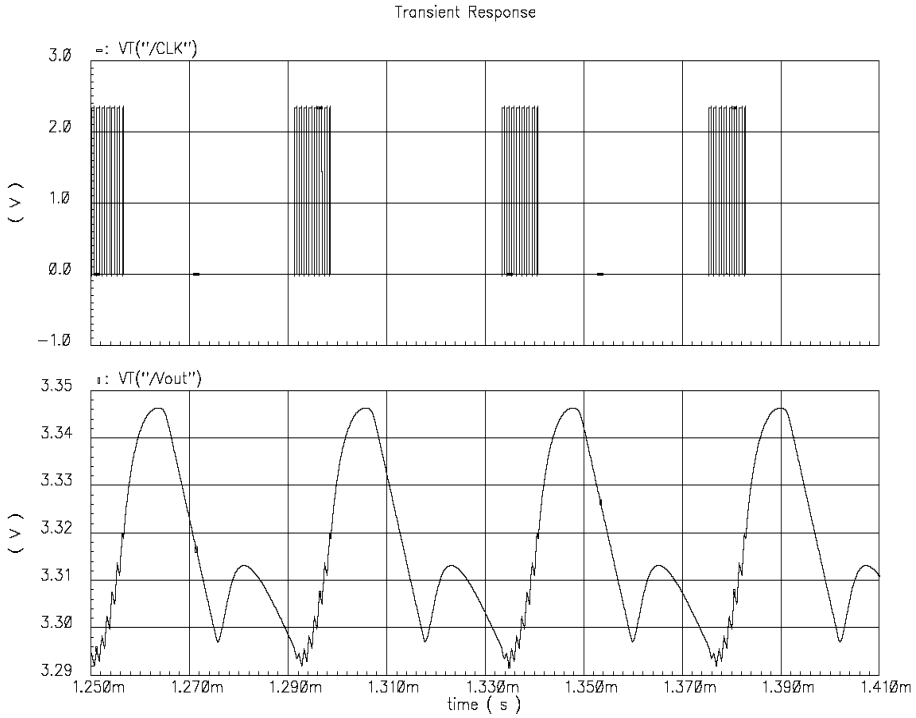

Fig. 21. Output ripple and CLK signal for $I_{out} = 10$ mA.

Of great importance are the values of the output current at which the converter switches in and out burst mode, because the power loss due to switching becomes prohibitively large only for low output currents. Working in burst mode for large output currents does not improve the efficiency; moreover it increases the output voltage ripple. Therefore, a pair of burst mode thresholds that do not significantly vary with the input voltage is preferred. In Fig. 22 the thresholds obtained using the MCC discussed above are presented. The threshold for entering burst mode is lower to ensure a hysteretic behavior.

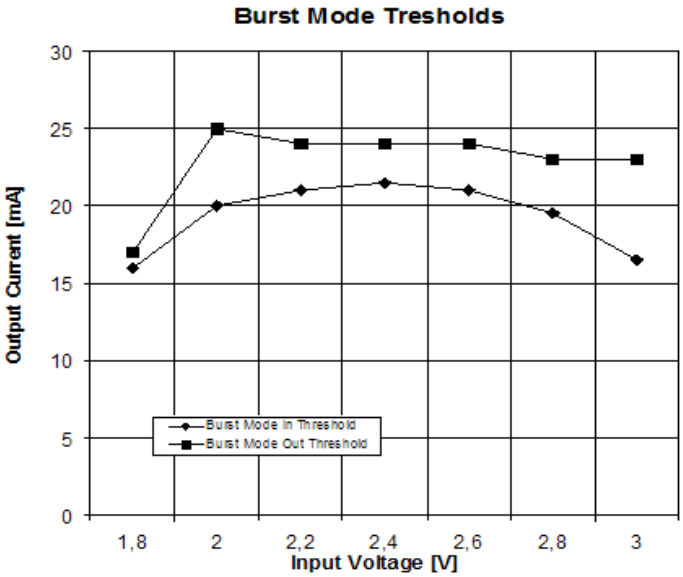

Fig. 22. Burst mode thresholds.

4. Conclusions

A SC DC-DC voltage converter is presented and its averaging small signal model was derived. The converter, designed using 0.18 um technology, is capable to deliver regulated, 3.3 V, low ripple output voltage for output currents up to 100 mA, and for input voltages in the range 1.8 V to 3.2 V. The converter is designed to automatically switch to burst mode when the output current decreases bellow a threshold. The mode control circuit used to detect the value of the output current and switch to one of the two possible modes of operation does not use inductors or resistive current sensors.

The model is based on the zero mean value of the currents passing trough the "fly" and "storage" capacitors. The model takes into account the conductance variation of a charge transfer control transistor as a function of the error amplifier output. A look-up table was used to update the control transistor conductance as a function of

the input voltage, voltage reference and the output load. It was found that the results obtained by running the model in Simulink fitted remarkably well to those obtained at transistor level simulations in Cadence.

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