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On Frequency and Quality Factor Independent Tuning Possibilities for RF Band-pass Filters with Simulated Inductors

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Abstract. A novel tuning principle for RF CMOS band-pass filter with simulated inductor allowing independent frequency and Q factor tuning is presented. The method makes use of a supplementary negative conductance and is sufficiently general to be applied to other active filters topologies as well. The proposed solution is intended to be used in the design of active multi-standard CMOS RF filters for mobile and network systems.

Key words: MOS simulated inductors, active RF multi-standard filters, frequency and Q-factor tuning, negative resistance.

1. Introduction

The growing market of wireless communications is a significant reason that motivates the study of new low cost and highly integrated architectures. In the last years much research has been devoted to the synthesis of active inductors, most of them grounded, due to their advantages over the passive counterpart. Indeed, spiral inductors are a critical issue in RF-design, their large on-chip area and weak quality factor being the main constraints for highly integrated products. Even though some methods for Q-factor enhancement in passive filters using on chip inductors have been proposed such as the use of negative resistances [1–2], active implementation of inductors is a challenging solution which has advantages like small chip area and high Q-factor and inductance values. Perhaps the most important advantage over their passive counterparts is the possibility of an easier frequency and Q-factor tuning

(automatic or programmable) the main drawbacks being higher power consumption, higher noise factor and poorer linearity all these being inherent in active topologies.

There are numerous topologies proposed and analyzed in literature for active inductors in CMOS technology in a frequency range up to a few GHz [3–11]. A reference paper for simulated inductors is [3] where a model for microwave applications is proposed.

Second order band-pass filters obtained using simulated inductors do not usually satisfy the wireless or even GSM RF filter requirements regarding bandwidth and sideband attenuation; higher order filters can be implemented by cascading second order structures [12] or improving the simulated inductor architecture by adding new transistors. A comparison between EGSM (Extended GSM) specs for RF filter and the second order active inductor performance are further presented to emphasize the difference.

2. The core topologies

Most BJT/FET/MOS active inductors models proposed in literature are based on capacitively loaded gyrators [13]. Since gyrators behave well only at low frequencies, for higher frequency applications transistors are used to simulate the inductance, their parasitic capacitors being used to emulate an inductive behavior.

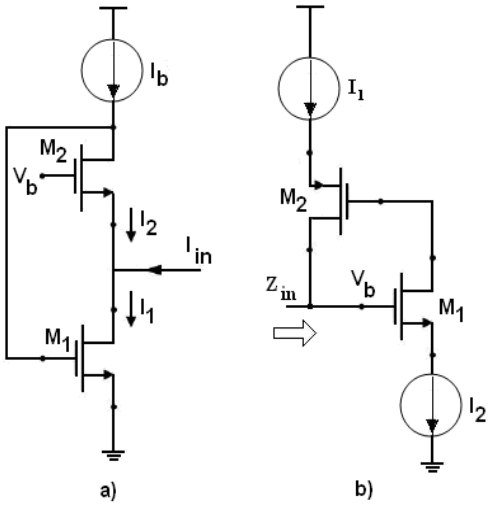

Fig. 1. CMOS active inductors reported in [4] (a) and [7] (b).

For gyrator based simulated inductors the inductance value can be changed either by modifying the load capacitors (varactors, switched-capacitors) or by changing the gyration resistance. However in a filter configuration based on gyrator simulated inductor, changing its value usually leads to changes in its central frequency and Q-factor. The same behavior occurs in the case of many transistor simulated inductors

RF filters. On the other hand, for filters designed for both EGSM and wireless standards it is important to have the facility of independently tuning the central frequency and the Q-factor in order to implement a multi-standard filter. This is the reason for researching architectures exhibiting independent tuning control for the above parameters.

In the following we briefly discuss the active filter architecture proposed in [4] and used in [5] as well (Fig. 1a). The equivalent small signal of this circuit is shown in Fig. 2. In order to get a more accurate description of the HF behavior of the circuit compared to that reported in [4] the output impedances of both MOS transistors have been taken into consideration in the following analysis where only the parasitic gate to drain capacitances were neglected.

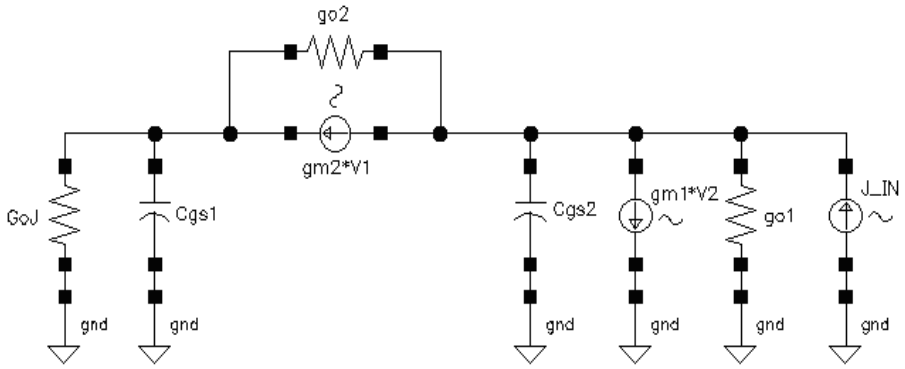

Fig. 2. Small signal model for the circuit in Fig. 1a.

In these conditions the input impedance of the circuit has the form:

$$Z_{in}(s) = \frac{b_1 s + b_0}{s^2 + 2\alpha s + \omega_0^2}, \tag{1}$$

where:

$$\omega_0 = \sqrt{\frac{g_{o2}g_{m1} + g_{m1}g_{m2} + g_{o1}g_{o2} + (g_{o1} + g_{o2} + g_{m2})G_{oJ}}{C_{gs1}C_{gs2}}}, \tag{2}$$

$$2\alpha = \frac{g_{m2}C_{gs1} + g_{o1}C_{gs1} + g_{o2}C_{gs2} + G_{oJ}C_{gs2} + g_{o2}C_{gs1}}{C_{gs1}C_{gs2}}, \tag{3}$$

$$b_1 = 1/C_{gs2};\ b_0 = (g_{o2} + G_{oJ})/C_{gs1}C_{gs2}. \tag{4}$$

Since both ω_0 and Q depend on all transistor parameters, it is obvious that an independent tuning is not possible.

Assuming that all transistor output impedances are infinite, the input impedance, ω_0 and the Q-factor become:

$$Z_{in} = \frac{\dfrac{1}{C_{gs2}}s}{s^2 + \dfrac{g_{m2}}{C_{gs2}}s + \dfrac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}, \quad \omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}, \quad Q = \sqrt{\frac{g_{m2}C_{gs1}}{g_{m1}C_{gs2}}}. \tag{5}$$

Relations (5) give errors of about 100–200 MHz for a central frequency of 700 MHz or higher. The consideration of transistor finite output impedance significantly diminishes these errors.

Another architecture shown in Fig. 1b and proposed in [7] has the small signal model presented in Fig. 3.

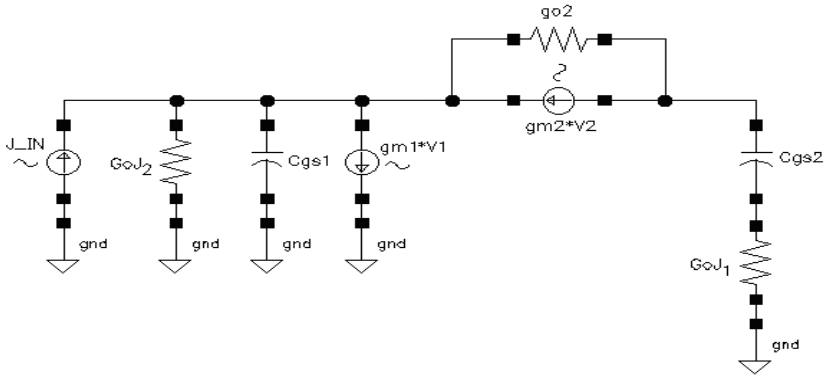

Fig. 3. Small signal model for the circuit in Fig. 1b.

It can be noticed that the small signal model is identical to that in Fig. 2, except for the presence of the output conductance of the current source I_1. However, in practical implementations, the place of this current source is changed as shown in the same reference so that, in fact, the small signal model presented in Fig. 2 is valid in this case as well. Consequently this active inductor is equivalent to that proposed in [4].

Other two active inductor configurations proposed in literature are given in Fig. 4.

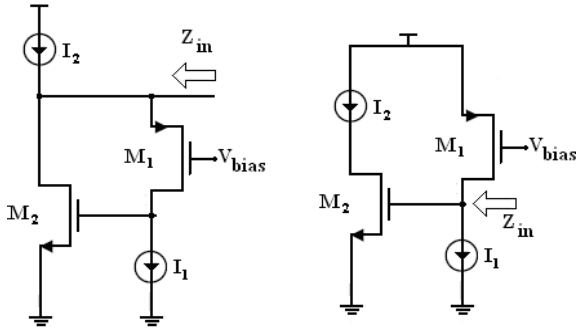

Fig. 4. CMOS active inductors proposed in [6] (a) and [10] (b).

The equivalent small signal models for both circuits shown in Fig. 4 are identical to that presented in Fig. 1 so they behave similarly.

The considerations presented above show that any active simulated inductor with two transistors has an input impedance of the form (1).

Regarding the small signal model, it can be easily shown that it actually represents a parallel RLC configuration as presented in Fig. 5.

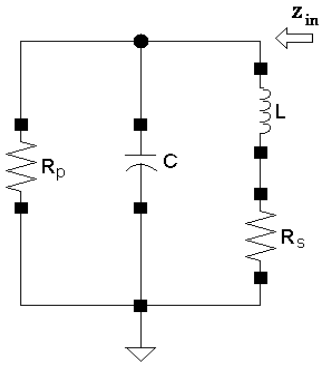

Fig. 5. Equivalent RLC resonator.

As mentioned above, inductors can be simulated using capacitively terminated gyrators. When the C_{gs} gate to source capacitance is used, an approximate value for the inductance is:

$$L \cong \frac{C_{par_{eq}}}{g_{m1}g_{m2}}, \tag{6}$$

where $C_{par_{eq}}$represents the equivalent parasitic capacitance given by a combination of C_{gs}, C_{ds} or C_{gd} and g_m, depending on the particular architecture for the simulated inductor. Practically, C_{ds} and C_{gd} have small values so in most cases only C_{gs} is considered. The series resistance R_s depends on the output resistances of the transistors and current sources which should be high enough. In this case the center frequency and quality factor are given by (5), where Q can be expressed as $Q = \dfrac{R_p}{\sqrt{L/C}}$.

An improvement for these configurations regarding the Q-factor can be obtained using a grounded negative resistance ($-R = -1/G$) connected to the input node of the active inductor. In this case, the new input impedance has the same general form (1) where ω_0 and 2α are:

$$\omega_0 = \sqrt{\frac{g_{o2}g_{m1} + g_{m1}g_{m2} + g_{o1}g_{o2} + (g_{o1} + g_{o2} + g_{m2})G_{oJ} - G(g_{o2} + G_{oJ})}{C_{gs1}C_{gs2}}}, \tag{7}$$

$$2\alpha = \frac{g_{m2}C_{gs1} + g_{o1}C_{gs1} + g_{o2}C_{gs2} + G_{oJ}C_{gs2} + g_{o2}C_{gs1} - GC_{gs1}}{C_{gs1}C_{gs2}}. \tag{8}$$

The above relations show that a change of the negative conductance will determine a change of both quality factor and center frequency. Besides, even though the

values of the output transistor conductances g_{o1} and g_{o2} are small compared to their transconductances, they still influence both the central frequency and the Q-factor as was seen from relations (5) and (6).

The quality factor improvement by using a negative resistance is useful both for low and high frequencies. The main problem in RF design is the quality of the negative resistance. A possible solution for the negative resistance implementation is the cross-coupled transistors architecture whose drawback it that of the parasitic capacitors which limits the frequency range. Even single transistor negative resistances still introduces parasitic capacitors.

In the followings we make several more considerations regarding the frequency response of the active inductor presented in Fig. 1a, with negative resistance (cross-coupled transistors). The simulated circuit is presented in Fig. 6, based on the core topology used in [5]. The frequency behavior is shown in Fig. 7 and Fig. 8, where the simulations were made for the GSM frequencies (900 MHz and 1800 MHz bands).

The above simulation results show that this architecture exhibit relatively high values for the Q factor, in this case $Q = 160$. This value allows a high attenuation for out-band frequencies which is the main requirement in designing wireless RF filters. It is important to mention that the tuning is possible for a high frequency range (about 1.5 GHz) just by changing I_b and V_b. A wider tuning range is possible by increasing the bias voltage which allows a higher bias current through the transistors.

In the followings, the above results are compared to the EPCOS specifications imposed to GSM filters for GSM bands (passive or SAW filters).

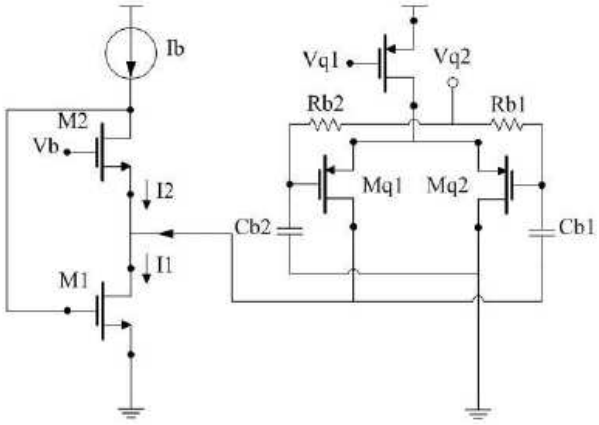

Fig. 6. Single–ended active RF band-pass filter with simulated inductor [5].

The main difference between active filters with simulated inductors and SAW passive RF filters is that the former do not allow higher bandwidths for certain attenuation. In other words, a second order band-pass filter can satisfy the requirements regarding the attenuation but not the bandwidth. Passive SAW filters are recognized as the best RF filters regarding the bandwidths and quality factors which can be

achieved. They allow high attenuation in a small bandwidth which is an advantage regarding the practical constraints imposed to wireless systems. The main drawback consists of their large size (a typical size is 2.5×2 mm) which is the main problem in implementing all on-chip RF transceivers. Moreover, all second order active band-pass filter configurations with simulated inductors are useless except for the case they are used for implementing higher order active filters in order to satisfy the in-band requirements (for example by cascading several second order cells).

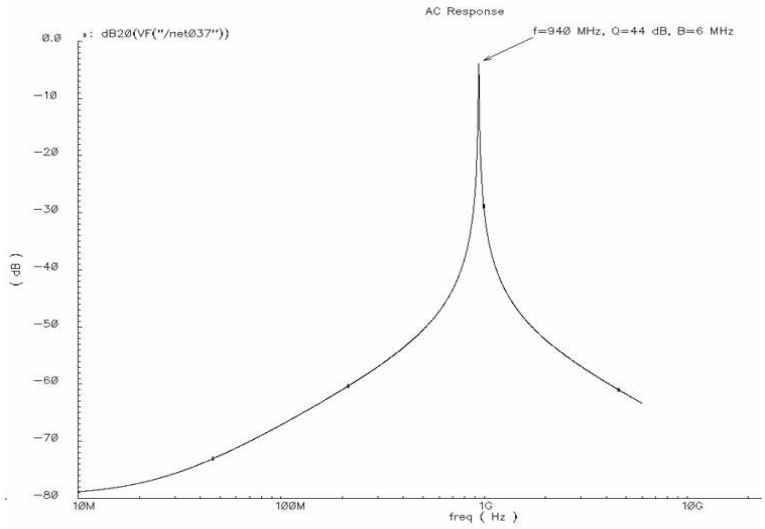

Fig. 7. Active RF filter with simulated inductor and Q–enhancement ($f_0 = 940$ MHz).

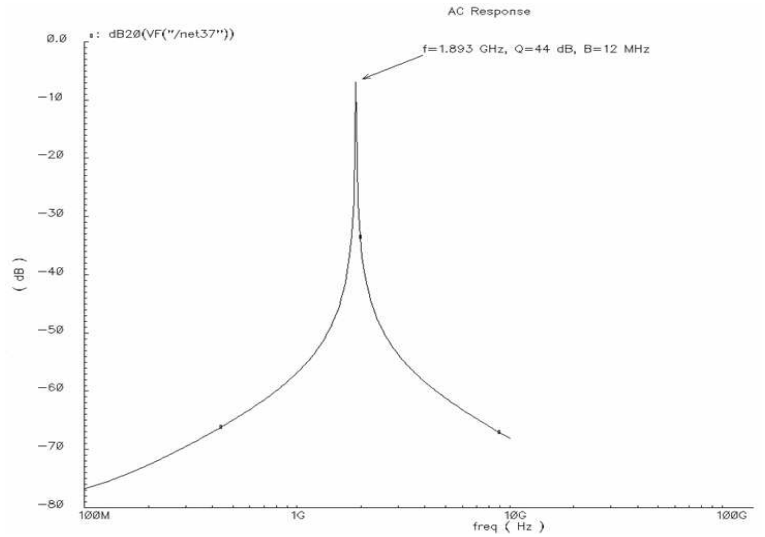

Fig. 8. Active RF filter with simulated inductor and Q–enhancement ($f_0 = 1893$ MHz),

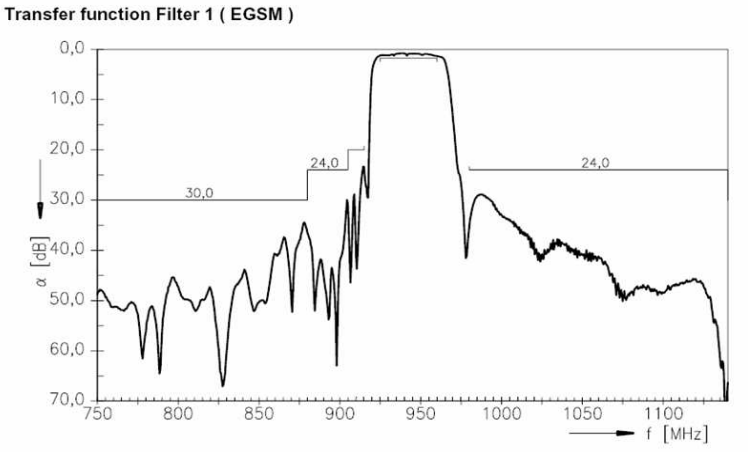

Fig. 9. GSM-900 RF filter specifications.

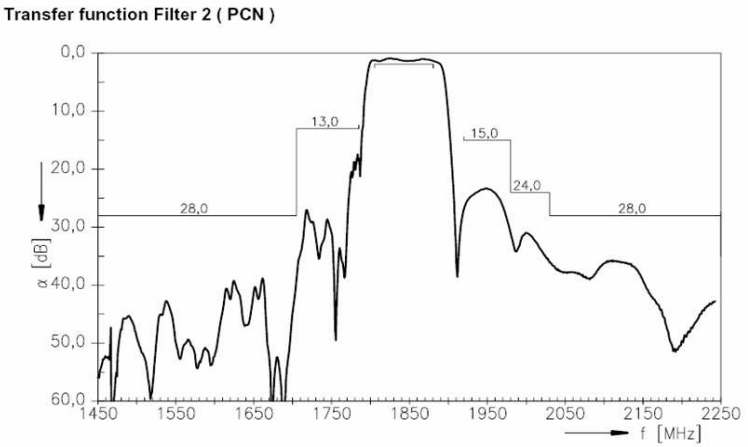

Fig. 10. GSM–1800 RF filter specifications.

In the following we discuss the possibility of implementing multi-standard active RF filters, i.e. the possibility of changing the bandwidth and center frequency in order to fulfill the requirements imposed by each standard. The first step in doing this is to implement an independent Q-factor and center frequency tuning architecture which is discussed in the following.

3. The proposed circuit

The use of a negative resistance presented above has the advantage of reducing the effect of parasitic for a lossy inductor, by minimizing the series resistance and the disadvantage of interdependencies between the Q and central frequency tuning.

The improved configuration consists in connecting an extra negative resistance to the second node and allows an independent tuning of the central frequency and quality

factor. Both negative resistances are dc decoupled which is a difference compared to all architectures using negative resistances, including VCOs, where they are dc coupled. The dc coupling contributes to the filter biasing and thus influences the frequency tuning. When decoupling the negative resistances a certain supplementary current is needed to be injected to the input node. This is easily done by interconnecting a new current source to the input node. The current source output impedance is supposed to be high enough so that it has no influence on the transfer function.

The core architecture used for implementing the independent tuning is that proposed in [4] and the proposed architecture is shown in Fig. 11.

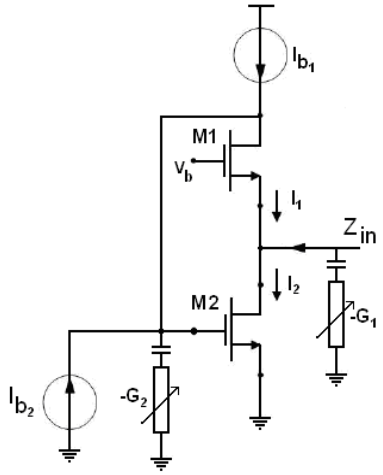

Fig. 11. Proposed solution for independent tuning.

In this case, the new $Z_{in}(s)$ is given by the same expression (1), where the coefficients are given in Table 1.

Table 1. Coefficients of $Z_{in}(s)$

Coefficient	Value
b_1	$1/C_{gs2}$
b_0	$(g_{o2} - G_2)/C_{gs1}C_{gs2}$
2α	$[(g_{m2} + g_{o1} + g_{o2} - G_1)C_{gs1} + (g_{o2} - G_2)C_{gs2})]/C_{gs1}C_{gs2}$
ω_0^2	$(G_1G_2 + g_{m1}g_{m2} + g_{o2}g_{m1} + g_{o1}g_{o2} - g_{o1}G_2 - G_2g_{m2} - g_{o2}G_1 - -g_{o2}G_2)/C_{gs1}C_{gs2}$

From Table 1 it is obvious that two methods to keep a constant ω_0 and tune the quality factor are possible.

The first one corresponds to $G_2 = g_{o2} = \text{ct.}$ when the influence of G_1 upon the center frequency is eliminated so the central frequency ω_0 is constant while Q will change with G_1 ("right" tuning). In this case, $b_0 = 0$ so this filter acts like an ideal integrator for low frequencies.

The second method, implies fulfillment of the relation $G_1 = g_{m2} + g_{o1} + g_{o2}$ (less easy to implement) so that the influence of G_1 upon the central frequency is rejected

– the central frequency ω_0 is constant while Q will depend on G_2 ("left" tuning). In this case, the dc gain will change in the same manner as G_2.

In other words, with the proposed configuration, the influence of either G_1 or G_2 upon the central frequency is eliminated and the tuning of Q can be achieved in two steps. First, suitable values of g_{m1}, g_{m2} and G_i (where i is either 1 or 2) satisfying one of the above discussed conditions are adopted in order to impose the desired central frequency. Next, a suitable value for G_j (where j is either 2 or 1) is chosen in order to change the quality factor. This will not affect the central frequency as far as G_j does not surpass certain limits. Since the negative resistances $-G_i$ are ac coupled they have no influence on the dc bias of the active filter, and thus on g_m as it happens in the case of the solutions proposed in [4], [5]. As shown above, in order to make this method feasible an extra current is needed to be injected to the input node of the filter.

Both resistances used so far in the above discussions were ideal; in the followings their parasitic capacitances are taken into account. Thus, a more suitable model for the proposed architecture is given in Fig. 12.

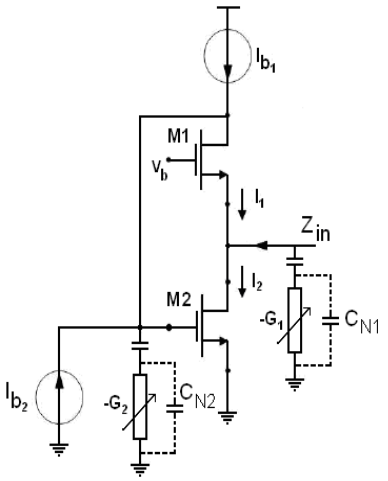

Fig. 12. Improved model for the proposed architecture.

For the above improved model the values of coefficients are given in Table 2.

Table 2. Coefficients for $Z_{in}(s)$

Coefficient	Value
k	$C_{gs1}C_{gs2} + C_{gs1}C_{N1} + C_{gs2}C_{N2} + C_{N1}C_{N2}$
b_1	$(C_{gs1} + C_{N2})/k$
b_0	$(g_{o2} - G_2)/k$
$2\alpha k$	$C_{gs1}(g_{o1} - G_1 + g_{m2}) + C_{N1}(g_{o2} - G_2) + C_{gs2}(g_{o2} - G_2) + C_{N2}(g_{m2} + +g_{o1} + g_{o2} - G_1)$
$\omega_0^2 k$	$G_1G_2 + g_{m1}g_{m2} + g_{o2}g_{m1} + g_{o1}g_{o2} - g_{o1}G_2 - G_2g_{m2} - g_{o2}G_1 - g_{o2}G_2$

Comparing the two architectures one can see that for the same desired frequency due to the presence of parasitic capacitors higher values for transconductances are expected. This will lead to higher power consumption and a more difficult biasing. Besides, the factor $2\alpha k$ has a higher value too, leading to a decrease of the quality factor. The algorithm of independent tuning still remains unchanged since the parasitic capacitors have no influence on $\omega_0^2 k^2$ but smaller quality factors than in the ideal case are obtained.

Even though the proposed architecture has several drawbacks as discussed before, the possibility of getting high quality factors still exists and this is proved by the simulation shown in Fig. 13.

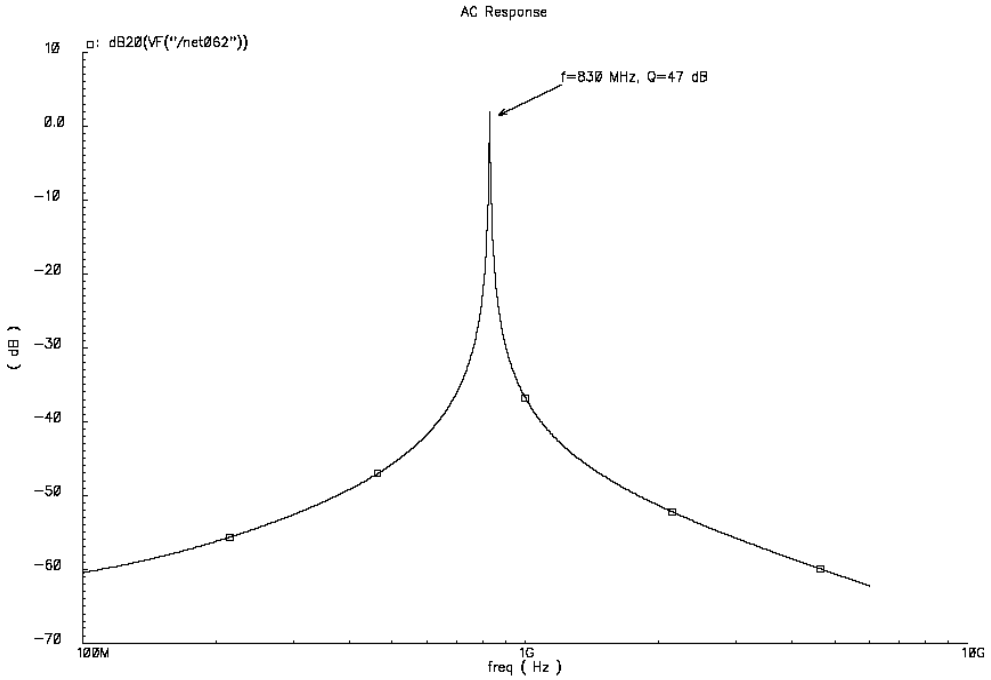

Fig. 13. High quality factor frequency response obtained with the architecture in Fig. 12.

The architecture proposed in Fig. 12 has been implemented using a modified version of the single ended negative resistance used in [5]. The previous resistance has been modified in order to let a current path to the ground. This negative resistance is represented in Fig. 14, the input node being the drain of transistor M_5.

The transistor M_5 ensures a dc path for M_1 and thus the equivalent circuit consists of a grounded positive resistance (due to M_5) in parallel to a negative one. However, for high frequencies, the parasitic capacitances associated to the negative conductance has to be taken into account but this fact has been found not to influence the presented tuning principle even though it lowers the filter central frequency.

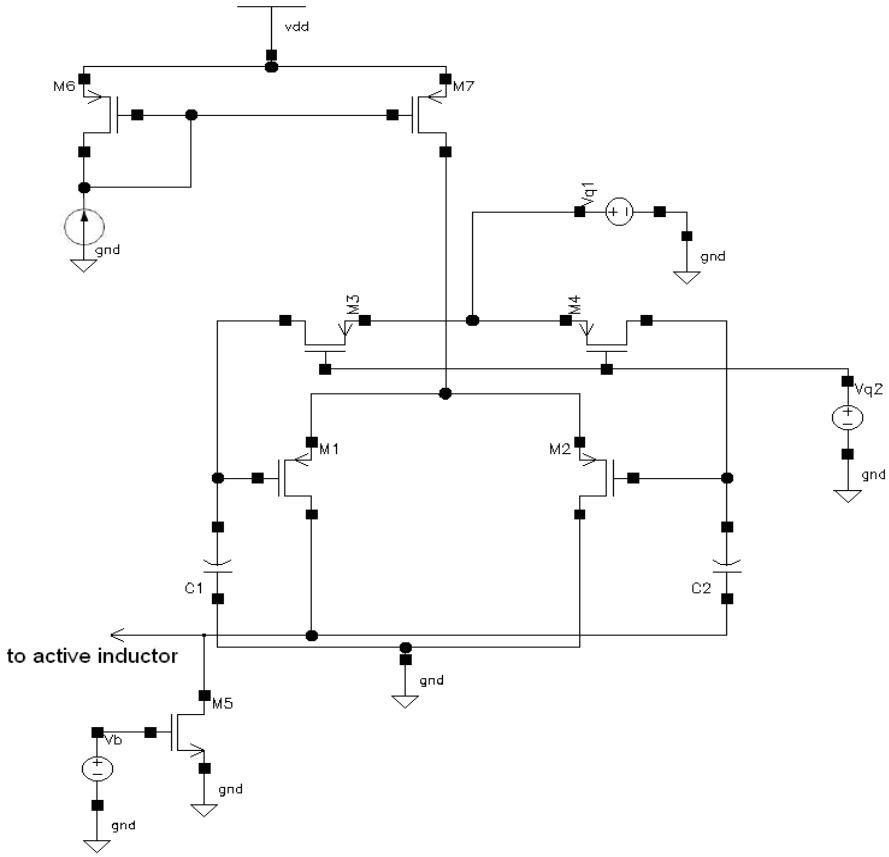

Fig. 14. Modified scheme for negative resistance.

4. Simulation results

A family of curves representing the frequency dependence of the gain for the architecture reported in [4] and [5] for various values of Q obtained by changing the negative conductance is presented in Fig. 15 where the frequency deviation may reach 50–60 MHz or more, depending on the value of the Q-factor.

The change of the central frequency is obvious. The results shown in Fig. 16 have been obtained using the circuit of Fig. 1b with ideal negative resistances for Q-tuning at three different frequencies (651 MHz, 869 MHz, 1.31 GHz).

In Figs. 17 and 18 the Q-tuning with "real" negative resistances implemented using the circuit in Fig. 3 at two frequencies 682 MHz and 686 MHz changing respectively the left and right negative resistances is presented. It has been found that the parasitic elements of the transistors lower the central frequency but the Q tuning does not change it when the discussed conditions are fulfilled.

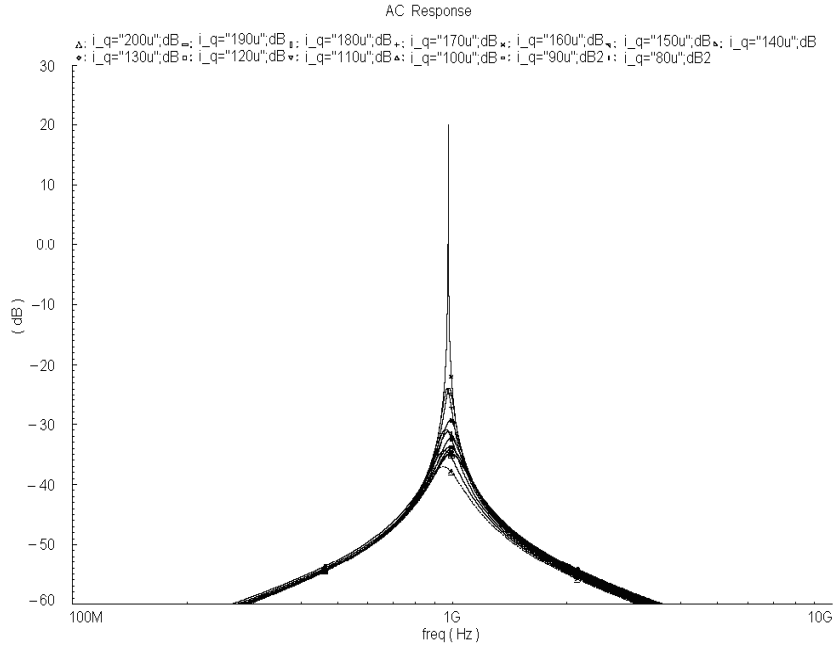

Fig. 15. *Q*-tuning for the core topology.

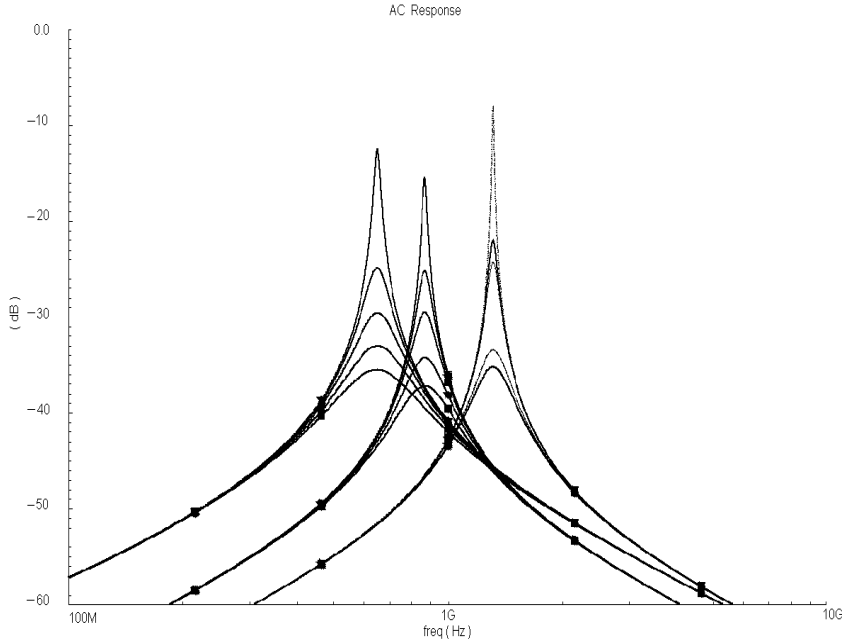

Fig. 16. *Q*-tuning with the proposed configuration at several frequencies.

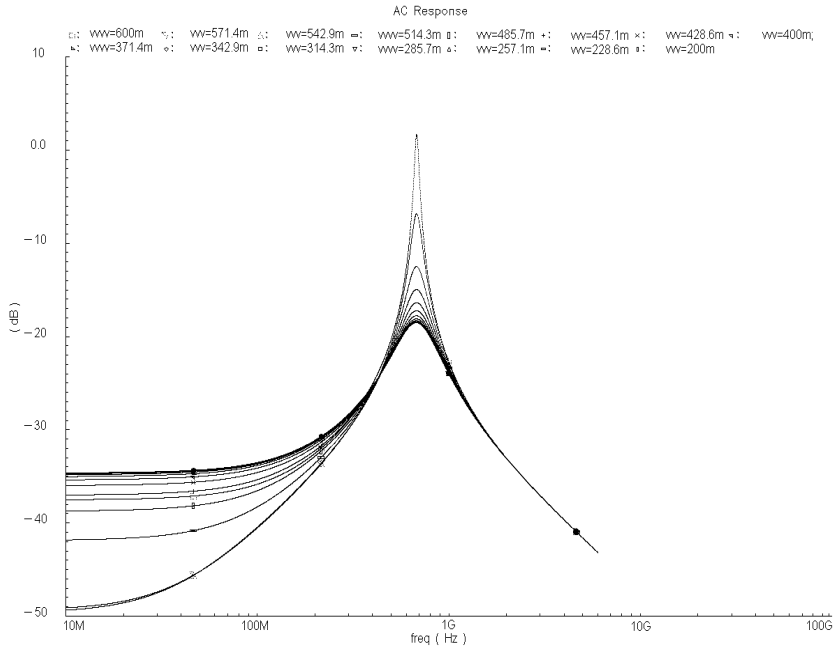

Fig. 17. Q factor left tuning ($f = 682$ MHz).

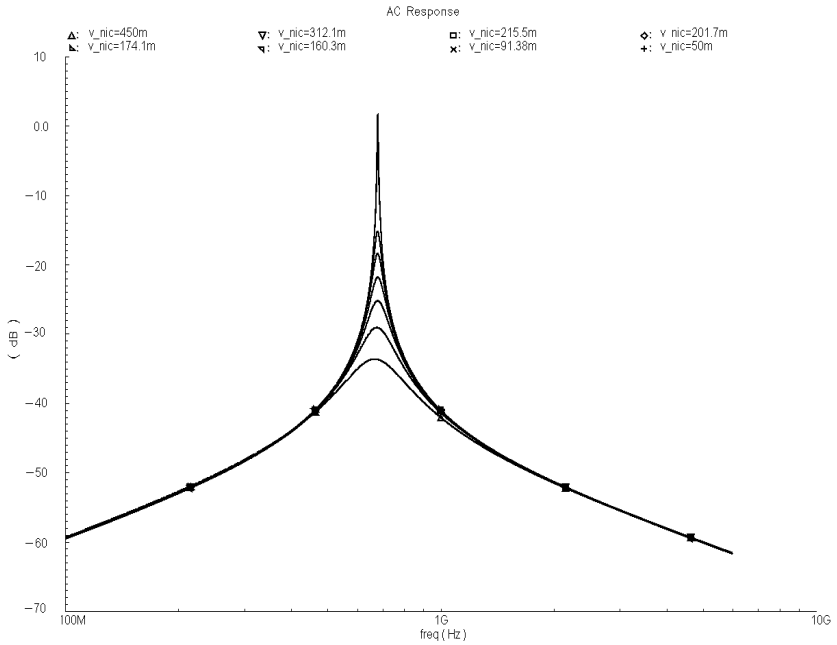

Fig. 18. Q factor right tuning ($f = 686$ MHz).

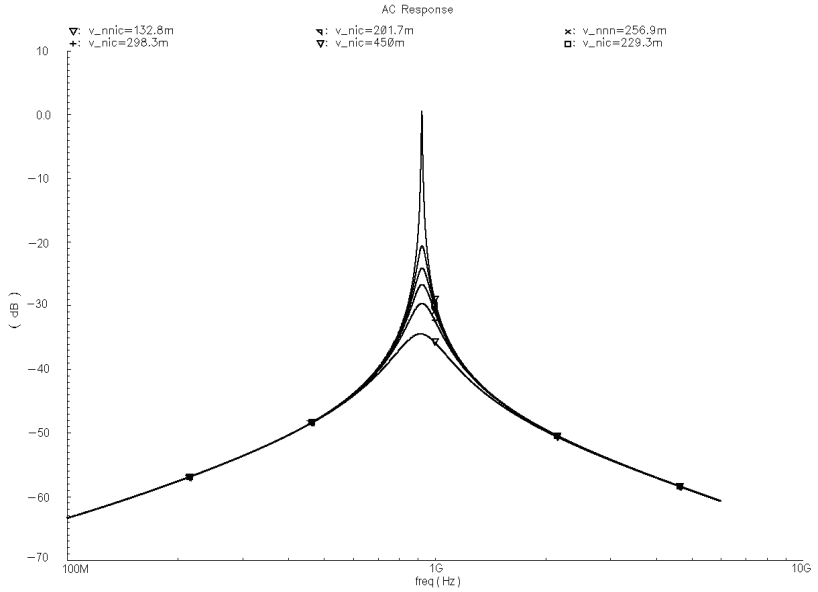

Fig. 19. Q factor tuning ($f = 920$ MHz).

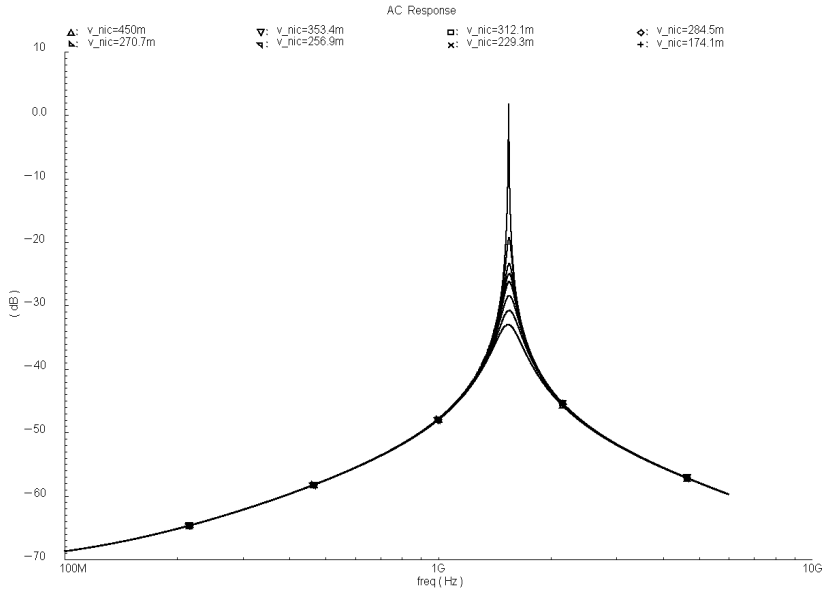

Fig. 20. Q factor tuning ($f = 1.54$ GHz).

The proposed configuration has been simulated for other two frequencies as well (the results are presented in Fig. 19 and Fig. 20). All simulations have been done in a 0.18 um technology.

4. Conclusions

A new approach for independent frequency and Q-factor tuning in a band-pass filter using simulated inductor has been presented. The method is based on the use of two negative resistances. Simulations showed that the parasitic capacitances of the negative resistances still allow independent tuning while slightly decreasing the maximum attainable central frequency. However it is important to ensure accurate values for the negative resistances otherwise the independent tuning is impossible.

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