

Design, Technology and Test of Micro-Machined Coplanar Grounded Wave-Guides on Si Substrates

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Abstract. Coplanar wave-guide grounded lines (CPWG) have been designed, realized by micro-machining of high resistivity silicon wafers and tested up to 40 GHz. Different configurations have been compared between them by changing the dimensions of the micro-machined via-holes used for the ground connection, as well as their number and separation, to get the optimal electrical matching conditions. Wide-band matching and losses as low as 0.1–0.2 dB/mm have been obtained within the 40 GHz range, in agreement with the predicted behavior.

Key-words: RF MEMS, micromachining.

1. Introduction

The utilisation of coplanar waveguide (CPW) configurations instead of the classical microstrips is chosen because it allows an easy shunt connection of the external elements in hybrid integrated circuits. Actually, the fabrication of monolithic integrated systems is compatible with typical CMOS processes.

Moreover, the CPW technology, is suitable of better integration and packaging with respect to the microstrip one [1–4]. Several improvements have been also proposed in literature for CPW micro-machined, trenched and SU-8 elevated structures [5–7].

Grounded CPW (CPWG) can be obtained by means of the metal backing of the substrate, connecting the upper ground planes to the bottom one by using via-holes. They can be achieved, depending on the substrate, by micro-drilling or laser processing for alumina, or by micro-machining for silicon and GaAs wafers. The utilization of CPWGs instead of CPWs can take advantage from: (i) wide-band matching, (ii) easier CPW-to-microstrip transition design for flange connector mounting, and (iii) improved ground definition for packaging purposes. In particular, the micromachining is an alternative technique with respect to the wire-bonding used in long CPW configurations, where the ground connection has to be renewed along the path by means of air bridge connections.

In this work, following the design given in [8], with care for the optimization of the electrical performances as a function of the via-holes number, separation and position, results about realization and test of CPWG configurations are presented. It is clearly demonstrated that the insertion losses can be improved, as predicted, up to frequencies as high as 30 GHz by using via-holes with respect to the same configuration without vias. The general arrangement used to model the exploited CPWG structures is shown in the following Fig. 1.

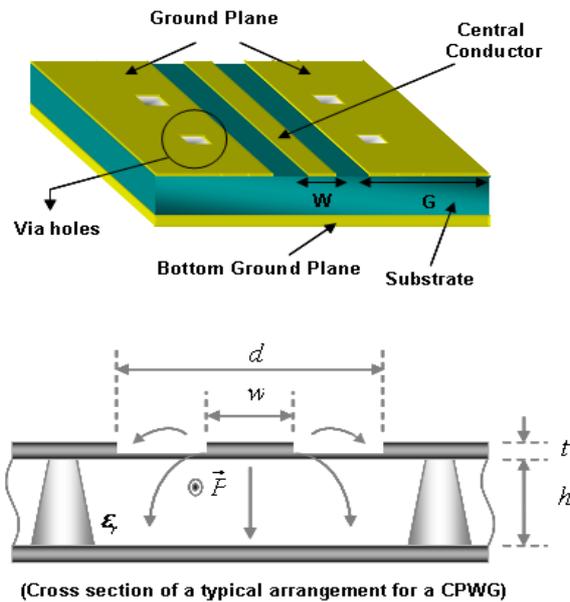


Fig. 1. Cross section of a CPWG. Via holes connect the lateral ground planes on the top side of the wafer to the bottom [9].

2. Technology of the CPWG

The manufacturing of the CPWG structures was based on photo-lithographic and chemical etching processes.

The process flow utilized for the realization of the structures is given in the following Table 1, where all the steps are described. Of course, the most critical step is the via hole realization, as the etching and the following metallization have to provide the proper electrical contact between the top side of the wafer, where the CPWG is defined, and the metalized bottom side. In particular, care has to be paid to the opening of the vias by means of the metal and thermal oxide removal steps.

The final cross section of the CPWG resulting from such a process is schematized in Fig. 2.

Table 1. Process flow for the realization of the CPWG structures. Si Wafers with thickness $400 \mu\text{m} \pm 20 \mu\text{m}$ and resistivity $\rho > 5000 \Omega \times \text{cm}$ have been used

<ol style="list-style-type: none"> 1. Thermal Oxidation 2. Cr/Au Deposition ($\text{Cr} \approx 100 \text{ \AA}$ / $\text{Au} \approx 4900 \text{ \AA}$) 3. Resist Spinning (Top Side) 4. Top Resist UV Exposure + Developer 5. Cr/Au Etching for CPWG Definition, and Resist Removal 6. Resist Spinning (Bottom Side) 7. Bottom UV Exposure + Developer 8. SiO_2 Etching on Bottom Side to open windows for KOH etching, and Resist Removal 9. KOH Chemical Etching on Bottom Side 10. SiO_2 Etching for complete opening of the via 11. Cr/Au Etching on the via only 12. Cr/Au Deposition on Bottom-Side for Ground Metallization
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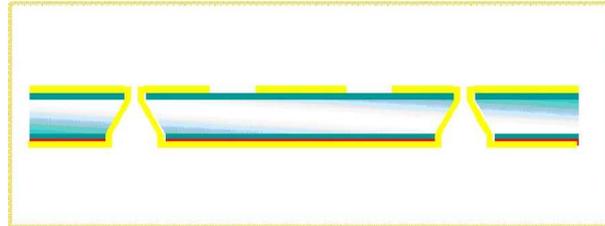


Fig. 2. Cross section of the CPWG obtained after the photo-lithographic and etching processes.

Because of the anisotropic chemical etching technique, the shape of the vias will be pyramid-like, with an angle of 54.7° , as shown in Fig. 3, where a photo of the via obtained by KOH chemical etching, before the metallization, is shown.

The structures to be realized are diagrammed in different orientations in the following Fig. 4.

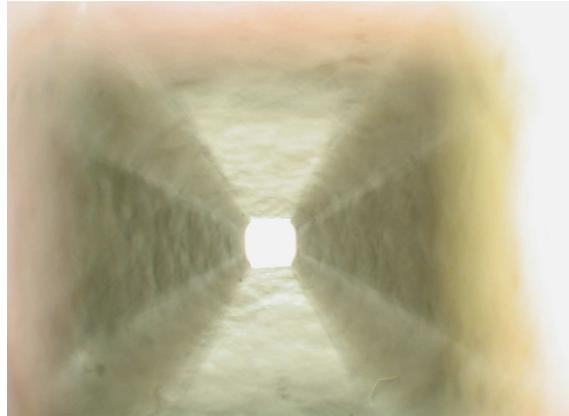


Fig. 3. Via hole realized by KOH etching on a 525 μm thick wafer, 755 \times 755 μm^2 large at the base and 11.5 \times 11.5 μm^2 on the top. A pyramidal section is obtained because of the (100) crystallographic orientation of the wafer substrate.

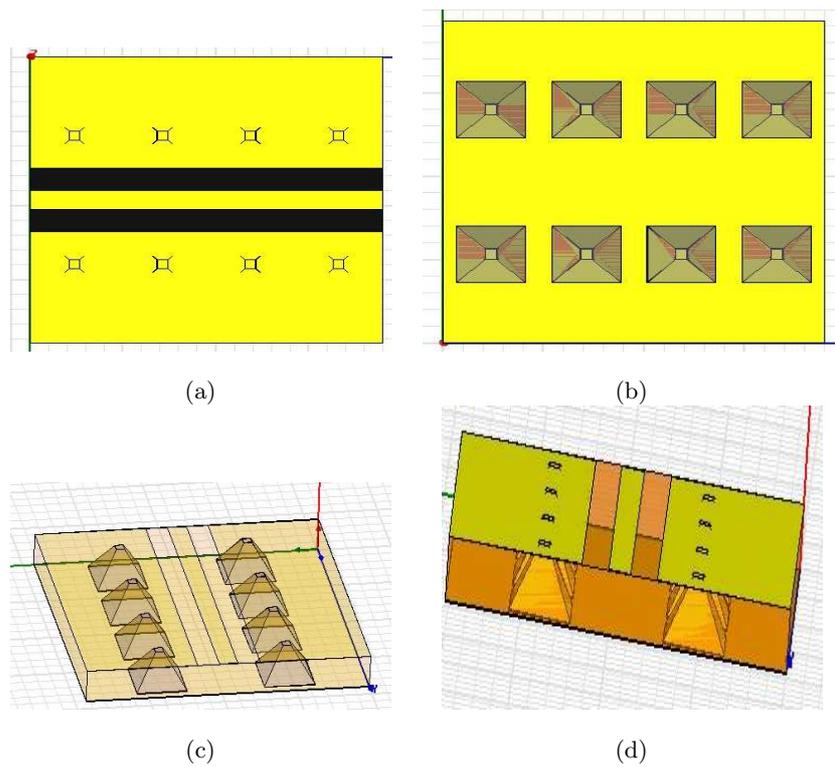


Fig. 4. Prospective views of the exploited CPWG structures: (a) top view, (b) bottom view, (c) and (d) tilted views with evidence for the 3D structure.

Preliminary simulations have been performed on CPWG configurations having one and two lines of vias, one close to the slot, and the second one in the middle or close to the external edge of the CPWG. Since no change in the S-parameters response has been predicted, as the dominant contribution is given by the line close to the slot [8], our technological efforts have been focused on a CPWG with one line of vias only. Examples of a single via hole, and four of them metalized after the KOH etching process are shown in Fig. 5 and in Fig. 6.

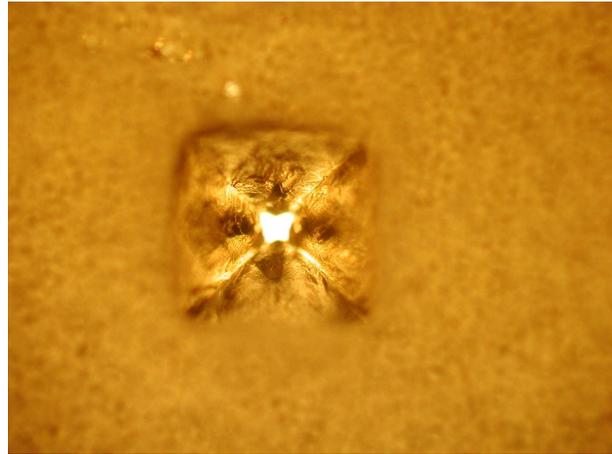


Fig. 5. Bottom view of a metalized via hole.

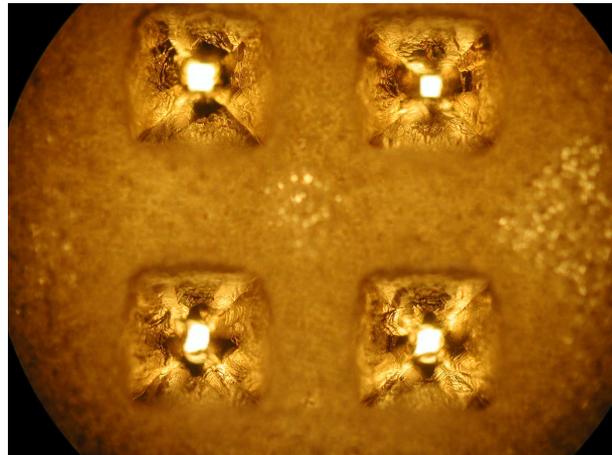


Fig. 6. Photo of the bottom side of a series of four metalized via holes.

By using a 400 μm thick silicon substrate, and a via hole of $684 \times 684 \mu\text{m}^2$ on the bottom side, accounting for the 54.7° angle due to the chemical etching, the top dimensions of the via will be $117.5 \times 117.5 \mu\text{m}^2$. The planar dimensions of the CPWG used for the experiment are given in Fig. 7, where, as an example, the configuration with a line of three via holes is given.

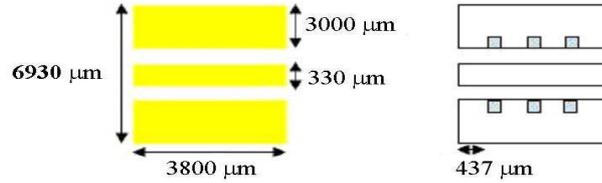


Fig. 7. Dimensions of the exploited CPWG lines. Example of the configuration with three via holes.

2. Simulations and measurements

Coplanar wave-guide structures on silicon wafers have been simulated by using the Ansoft HFSS 3D-module. In particular, 400 μm thick high resistivity, thermally oxidized (100)-oriented silicon wafers have been considered, with 1 μm of SiO_2 thermally grown. The conductivity imposed for Si is $\sigma = 0.02 \text{ S/m}$, and the dielectric constant is $\epsilon_r = 11.9$, while the dielectric loss tangent is $\tan \delta = 0.002$. For SiO_2 , $\epsilon_r = 4$ was used. The metallization, made by Cr/Au, was considered to have a thickness of 0.5 μm and $\sigma = 4.1 \times 10^7 \text{ S/m}$. Following literature results [10], the via holes should be far each other at least a distance $\lambda/20$, and each via far from the external edge of the CPWG for a distance which is at least one diameter of the via itself. The exploited structures are diagrammed in the following Fig. 8.

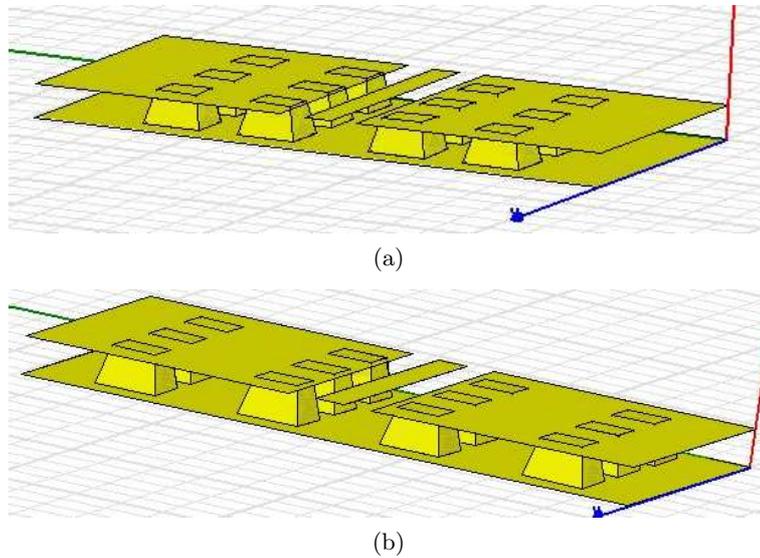


Fig. 8. Simulated CPWG with two lines of via holes, with the first line close to the slot and the second one (a) in the middle of the lateral ground plane, and (b) close to the external edge.

Simulations for the CPWG for one of the most promising configurations, with 3, 4 and 5 holes placed along the length of the device are shown in Fig. 9, and compared with the structure with no via holes.

As a result from the comparison with other structures having different number of vias and dimensions, it turns out that no significant enhancements of the matching conditions are obtained when larger holes are considered, and especially for frequencies higher than 10 GHz no improvement is observed [8].

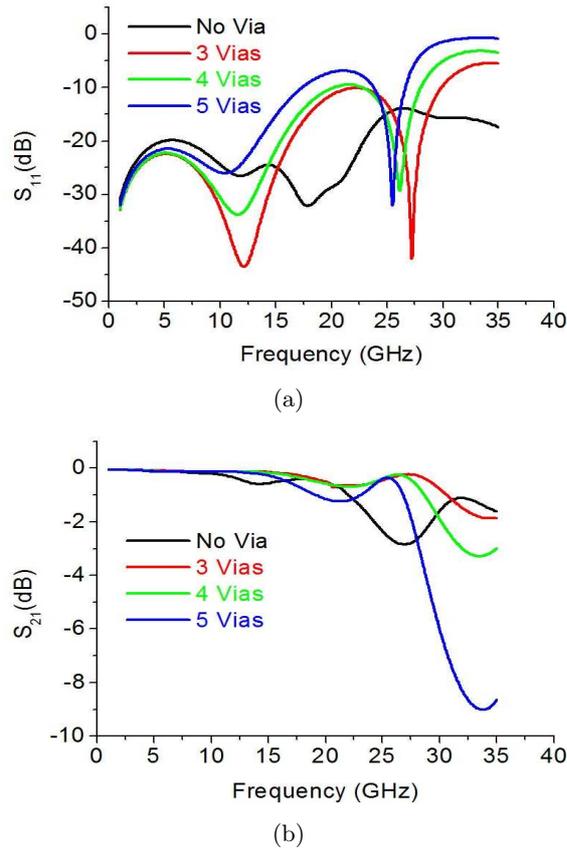


Fig. 9. Simulated response for the CPWG on 400 μm thick substrate with 3, 4 and 5 vias and $684 \times 684 \mu\text{m}^2$ area on the bottom side of the wafer.

Moreover, the best results are obtained when the vias are realized close to the slot, as evidenced by the predictions given in Fig. 10, where the structure has been simulated by placing the vias in the middle of the lateral ground of the CPWG and close to the external edge of it. Actually, resonances appear when the vias are far from the slot.

The experimental results on the realized structures are shown in Fig. 11, where the scattering parameters, measured by means of an on-wafer probe station, are plotted.

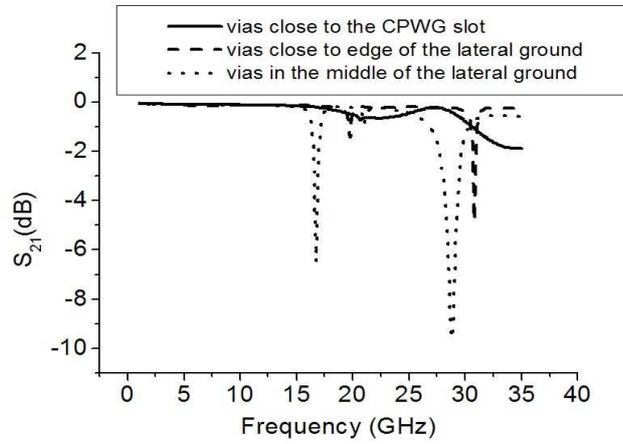


Fig. 10. Transmission parameter for the CPWG on a 400 μm thick wafer. The best performances are obtained when the vias are close to the slot.

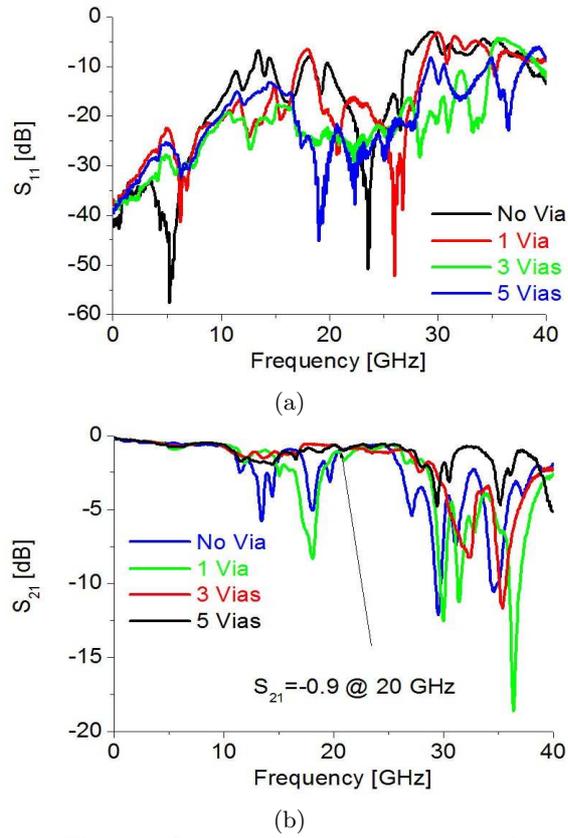


Fig. 11. Scattering parameters measured on a 1, 3 and 5 vias structure.

3. Conclusions

Coplanar wave-guide grounded configurations (CPWGs) have been studied for wide-band matched interconnections suitable of better ground definition and packaging. Technology has been set up to obtain the structures on micro-machined silicon high resistivity wafers (100)-oriented. The predicted in-band response is in quite good agreement with the trend of the experimental findings, especially in the frequency range used to optimize their electrical performances, and wide-band characteristics have been obtained up to 30 GHz. It has to be stressed that the periodic distribution of the holes is a limitation when a very wide-band response is required. In fact, the $\lambda/4$ -resonances could appear dependently on the imposed distance between the holes. An alternative solution with respect to the proposed configurations is the realization of non-periodic holes, with some design complications followed by enhanced performances from the wide-band response point of view. Work is in progress for optimizing the technology and the design procedure for the exploited structures.

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