

Design of Robust RF-MEMS Phase Shifters in Ka-band

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Abstract. Design and performance of RF-MEMS Phase Shifters in Ka-band are presented. The used Si compatible technology aims to fabricate RF-MEMS devices which are able to handle medium RF-power. Two Phase Shifter versions were designed and compared with respect to capacitance fluctuations.

Key words: RF-MEMS, Phase Shifters, Switched-Line, Loaded-Line, Ka-Band.

1. Introduction

RF phase shifters are essential building blocks for phased array antennas in telecommunication and radar applications. To reduce cost and power dissipation and improve RF performance of such applications, currently much research about MicroElectroMechanical (MEM) switch integration (as opposed to an active approach) is done. The use of MEMS in these blocks presents important challenges. One of them is to obtain robust circuits. In this paper is shown which architecture to choose in order to minimize the effect of RF-MEMS capacitance fluctuation.

We present the design and performance of RF-MEMS phase shifters in the Ka-Band. Two versions of the phase shifters have been designed. The results are shown and compared in this paper.

2. Technology

The microphotograph of the used RF-MEMS is presented in Fig. 1. The switch is made of a $50\ \Omega$ coplanar wave guide over which a movable metallic membrane is placed in a distance of $3\ \mu\text{m}$. The MEM bridge includes two main components:

- the bridge that exhibits two different capacitances in the up and down state,
- two actuation electrodes that are located apart in order to attract the bridge to the CPW line through an electrostatic force.

A $0.25\ \mu\text{m}$ thick Silicon Nitride dielectric layer is placed just between the movable bridge and the coplanar line to avoid any short-circuits.

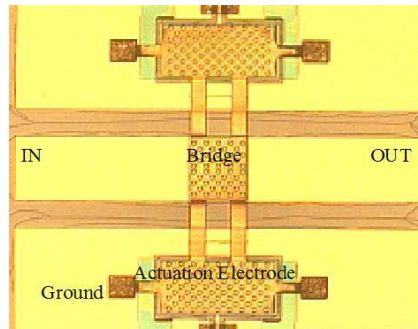


Fig. 1. RF-MEMS microphotograph.

The RF-MEMS technology is developed on silicon substrates covered by a $20\ \mu\text{m}$ thick BenzoCycloButene (BCB) layer. This polymer is compatible with above IC post-processing. The main fabrication steps are described in [1].

Electrical measurements up to 30 GHz in up and down state are presented in Fig. 2.

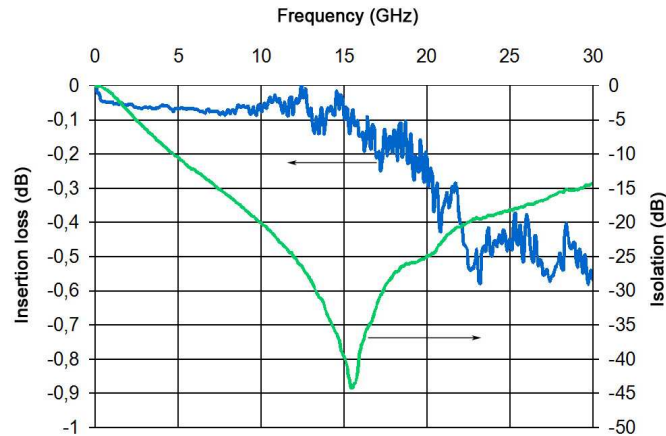


Fig. 2. Transmission parameter of RF-MEMS devices in up and down position.

The switch has a very low insertion loss of 0.25 dB (including access lines) at 20 GHz (which is the design frequency for the phase shifters) and a high isolation of 25 dB at the same frequency in off-state. The excellent results validate the technology and give as well attracting prospects for RF-MEMS based circuits in terms of performance. An actuation voltage of 25 V is required to collapse the membrane on the line.

We have built, from measurements, an electrical equivalent schematic (Fig. 3) in Agilent ADS (Advanced Design System) which takes into account the technological variations and will be used for circuit design.

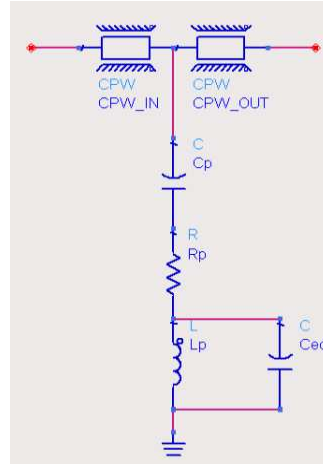


Fig. 3. MEMS electrical equivalent schematic.

The bridge capacitance $C_{p(\text{REF})}$ is defined by the bridge area ($160 \times 200 \mu\text{m}^2$ in Fig. 1). $C_{p(\text{REF})}$ is 90 fF in up state and 2900 fF in down state.

3. Design

We have designed two versions of 1-bit phase shifters: a switched-line and a loaded-line. For each version, two circuits have been realized: the first one provides phase shift of 22.5° and the second one 45° . All circuits use shunt switches and 50Ω ground coplanar waveguides. They have been optimized at 20 GHz.

3.1. Switched-line phase shifter

The switched-line phase shifter [2] is based on an original SPDT (Single Pole Double Throw) switch. The phase shift $\Delta\Phi$ results from electrical length difference between the top line and the bottom line (i.e. Δl). The circuit (Fig. 4) is composed of 4 standard RF-MEMS and 4 up state blocked RF-MEMS (MEMS_{up}).

The original SPDT structure [3] that we use takes advantage of the OFF-state switch capacitance to realize a semi-distributed quarter wave line. This provides a transformation from the closed switch short circuit to an open circuit at the input.

The impedance inverter [4] is constituted by a short high characteristic impedance line, which acts as a semi-distributed inductance surrounded by two MEMS capacitors, which satisfy these two equations:

$$Z = Z_0 \sin \theta \quad (1)$$

$$\omega C_{p(\text{up})} = (1/Z_0) \cos \theta, \quad (2)$$

where Z_0 is the characteristic impedance of the quarter-wavelength line, Z the characteristic impedance of the shortened line, θ the electrical angle of the shortened line, and ω the angular frequency.

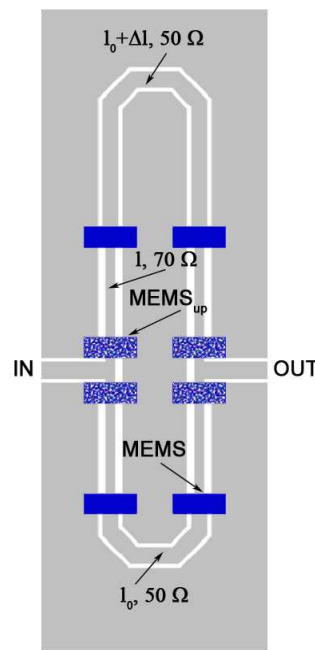


Fig. 4. The 1-bit SPDT switched-line phase shifter.

So, a higher 70Ω characteristic impedance for line 1 has been adopted. As mentioned previously, two 1-bit switched-line phase shifters have been designed. They only differ by the value of Δl . The phase delay is 22.5° in the first and 45° in the second circuit.

3.2. Loaded-line phase shifter

Also, a Class III loaded-line phase shifter has been designed. It uses 2 RF-MEMS. Figure 5 presents the phase shifter topology.

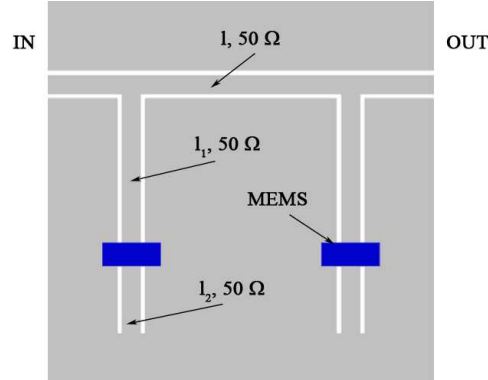


Fig. 5. The 1-bit Class III loaded-line phase shifter.

In the loaded-line phase shifter, the principal line 1 is connected likewise to one of two different loads that provide the desired phase difference. A Class III topology [5] has been chosen because it presents a constant loss per phase bit, and a relatively wideband constant-phase response. In this case, the stub lengths are calculated by these equations:

$$\theta = 90^\circ, \quad (3)$$

$$\theta_1 = \tan^{-1}(B_1/Y_s), \quad (4)$$

$$\theta_2 = \tan^{-1}(B_2/Y_s) - \theta_1, \quad (5)$$

$$B_1 = -B_2 = Y_0 \tan(\Delta\Phi/2), \quad (6)$$

where θ is the electrical angle of the line 1, θ_1 the electrical angle of the line l_1 , θ_2 the electrical angle of the line l_2 , B_1 and B_2 are the complex-conjugate loading susceptances, Y_s the characteristic admittance of the stub line, and $\Delta\Phi$ the phase shift.

Two 1-bit Class III loaded-line phase shifters have been designed. They differ by the value of complex-conjugate stub line lengths (l_1 , l_2). The phase delay is 22.5° in the first and 45° in the second one.

4. Results

Designs have been developed by ADS schematic simulations and confirmed by HFSS electromagnetic simulations.

4.1. First comparisons

In this part, comparisons between the switched-line and the loaded-line phase shifters are shown and analyzed. Three parameters are studied versus $C_p/C_{p(\text{REF})}$ at 20 GHz: phase shift, return loss and insertion loss.

We can see in Fig. 6 that phase shift $\Delta\Phi$ is similarly good for the two 22.5° versions.

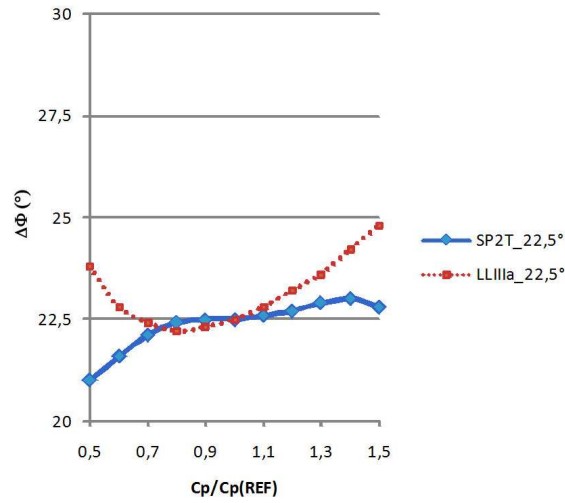


Fig. 6. Phase shift *versus* $C_p/C_{p(REF)}$ at 20 GHz for 22.5° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

However, for the 45° versions (Fig. 7), the switched-line phase shifter has a smaller phase deviation. Indeed, its phase shift is constant between 0.7 and 1.3 whereas the phase shift of the loaded-line strongly increases with $C_p/C_{p(REF)}$.

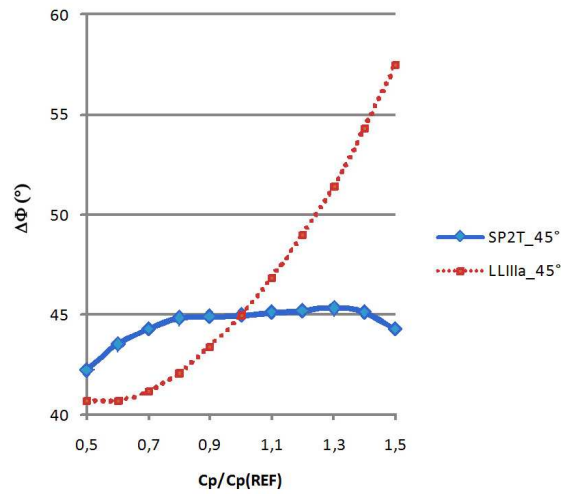


Fig. 7. Phase shift *versus* $C_p/C_{p(REF)}$ at 20 GHz for 45° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

The analysis of the return loss, for $C_p/C_{p(REF)} = 1$, shows S_{11} equals -33 dB in the 22.5° switched-line version and -21 dB in the 22.5° loaded-line (Fig. 8).

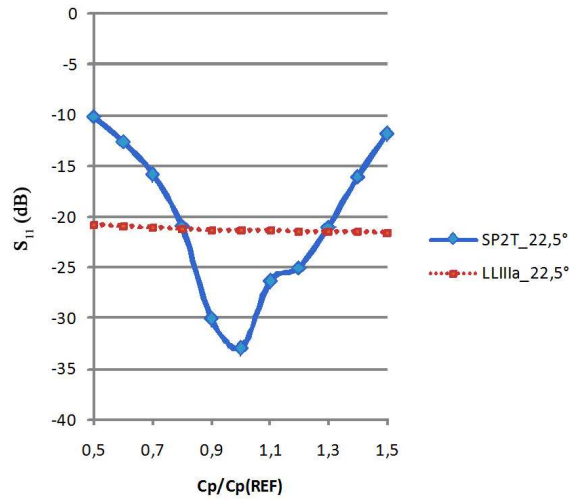


Fig. 8. Return loss *versus* $C_p/C_{p(REF)}$ at 20 GHz for 22.5° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

For $C_p/C_{p(REF)} = 1$, the return loss is -28 dB in the 45° switched-line version and -21 dB in the 45° loaded-line version (Fig. 9). We can note a return loss below -21 dB for the switched-line version around $C_{p(REF)}$ from 0.8 to 1.3. At the other hand, the return loss of the loaded-line is more broad-band. In general, the loaded-line presents an excellent response for the 22.5° small phase delay.

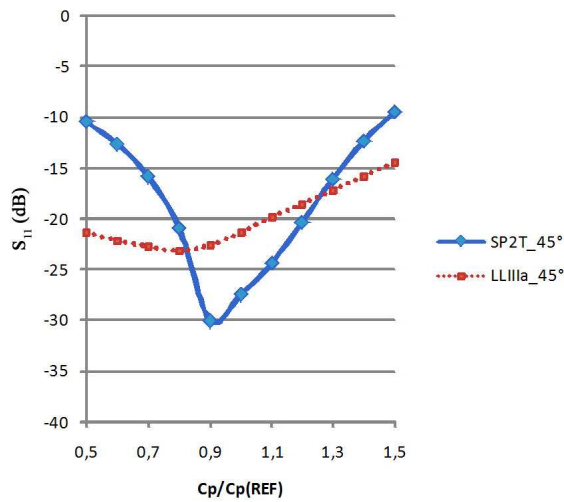


Fig. 9. Return loss *versus* $C_p/C_{p(REF)}$ at 20 GHz for 45° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

Now, let us examine the insertion loss S_{21} . For $C_p/C_{p(REF)}=1$, the insertion loss is -1.1 dB in the 22.5° switched-line version and -1.3 dB in the 22.5° loaded-line (Fig. 10). For $C_p/C_{p(REF)} = 1$, the insertion loss is -1.2 dB in the 45° switched-line version and -1.4 dB in the 45° loaded-line (Fig. 11). In both cases, the switched-line yields an insertion loss about 0.2 dB below.

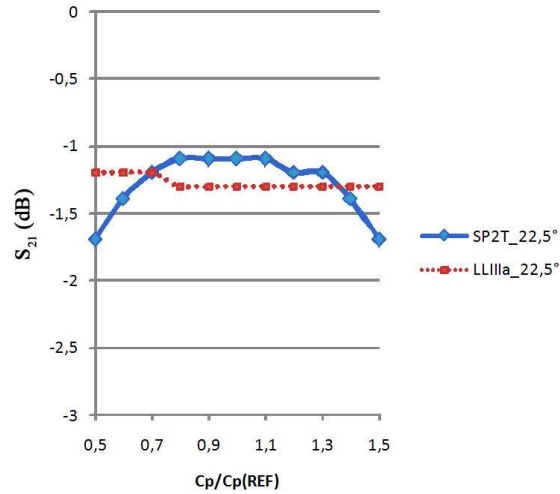


Fig. 10. Insertion loss *versus* $C_p/C_{p(REF)}$ at 20 GHz for 22.5° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

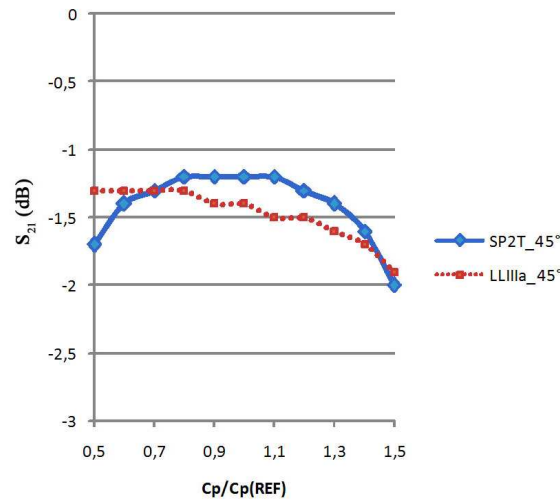


Fig. 11. Insertion loss *versus* $C_p/C_{p(REF)}$ at 20 GHz for 45° switched-line (SP2T) and loaded-line (LLIII) phase shifters.

On the one hand, we can conclude that for small phase shifts, the loaded-line version is interesting by its simplicity and performance.

On the other hand, for a 45° phase shift (and above), the switched-line version is advantageous by its constant phase despite of RF-MEMS capacitance fluctuation.

4.2. Further results

In this sub-section, dispersions are described and explained. Furthermore, new comparisons and results are presented.

The capacitance dispersion comes from two main fluctuations:

- The first one concerning the up-state capacitance and
- The second one concerning the down-state capacitance.

The **up-state capacitance** [6] of the RF-MEMS is:

$$C_{up} = \frac{\varepsilon_0 \times A}{g + \frac{t_d}{\varepsilon_r}}, \quad (7)$$

where ε_0 is the vacuum dielectric constant, A the capacitive area of the bridge, g the air gap between the dielectric and the bridge (Fig. 12), t_d the dielectric thickness and ε_r the relative permittivity.

So, the up-state capacitance depends on the bridge height g which is defined by the bridge stiffness and the photoresist releasing.

The **down-state capacitance** is:

$$C_{down} = \frac{\varepsilon_0 \times \varepsilon_r \times A}{t_d}. \quad (8)$$

So, the down-state capacitance depends on the thickness of the dielectric.

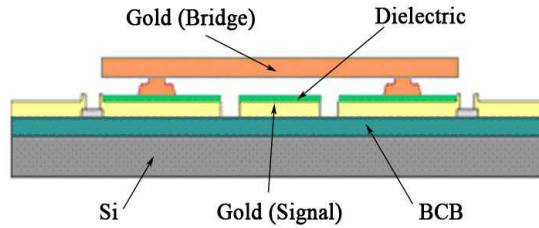


Fig. 12. RF-MEMS cross section.

Using (7) and (8), the $C_p/C_{p(\text{REF})}$ ratio can be calculated:

-in up-state

$$C_p/C_{p(\text{REF})_{up}} = \frac{g\varepsilon_r + t_d}{(g + \Delta g)\varepsilon_r + t_d + \Delta t_d}; \quad (9)$$

Thus, with $g \gg t_d$, i.e. if the dielectric thickness is much smaller than the air gap:

$$C_p/C_{p(\text{REF})_{\text{up}}} \approx \frac{1}{1 + \Delta g/g}; \quad (10)$$

-in down-state

$$C_p/C_{p(\text{REF})_{\text{down}}} = \frac{1}{1 + \Delta t_d/t_d}. \quad (11)$$

In practice, if $\Delta g \approx \Delta t_d \approx \Delta h$ and $g \gg t_d$, the ratio can be approximated by:

-in up-state

$$C_p/C_{p(\text{REF})_{\text{up}}} \approx 1, \quad (12)$$

-in down-state

$$C_p/C_{p(\text{REF})_{\text{down}}} \approx \begin{cases} < 1 & \text{for } \Delta h > 0, \\ > 1 & \text{for } \Delta h < 0. \end{cases} \quad (13)$$

For example, in our RF MEMS technology, for $\Delta h = 0.1 \mu m$, the $C_p/C_{p(\text{REF})}$ ratio is equal to 0.98 in up-state and 0.71 in down-state.

From previous equations, we can conclude that down-state capacitance fluctuations are more important than up-state capacitance fluctuations.

Also, another parameter has to be considered: the roughness of the signal dielectric surface [7, 8]. It plays a critical role in down-state. Indeed, the dielectric surface isn't completely smooth. The atomic force microscopy (AFM) measurement (Fig. 13) shows this. So, the contact between the dielectric and the bridge in down-state is reduced and provides lower capacitance. Thus, this is another reason that the down-state capacitance dispersion is higher.

N.B. : The dielectric roughness is directly proportional to CPW roughness.

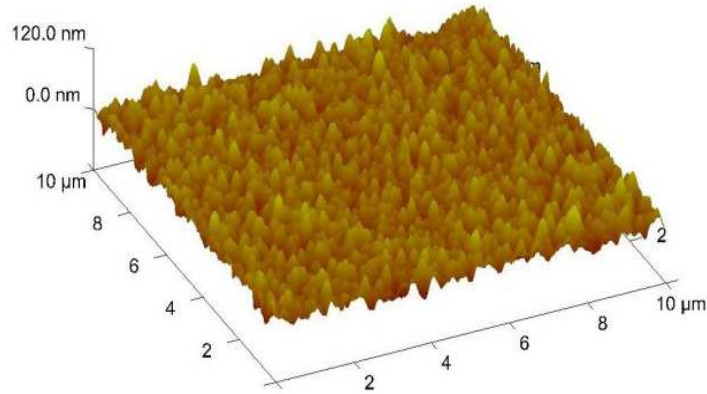


Fig. 13. Roughness of the signal dielectric surface.

Now, let us consider differences between the C_{up} and C_{down} dispersions on the two designed phase shifter versions. When analyzing C_{up} dispersion, $C_p/C_{p(REF)down}$ is fixed at 1 and when analyzing C_{down} dispersion, $C_p/C_{p(REF)up}$ is fixed at 1.

For a 22.5° phase shift (Fig. 14), the two responses are relatively correct but we can note that, for the loaded-line version, the up-state dispersion leads to $C_p/C_{p(REF)up}$ above 1 whereas the down-state dispersion yields a $C_p/C_{p(REF)down}$ below 1.

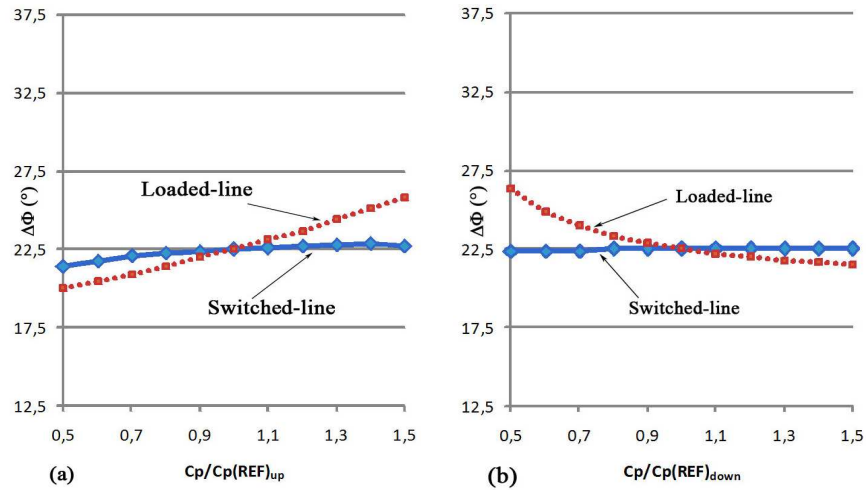


Fig. 14. C_{up} (a) and C_{down} (b) dispersions for 22.5° switched-line and loaded-line phase shifters.

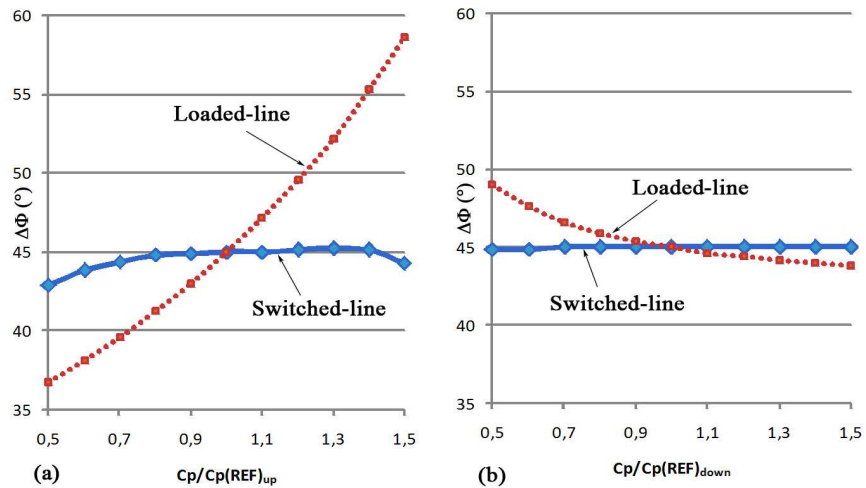


Fig. 15. C_{up} (a) and C_{down} (b) dispersions for 45° switched-line and loaded-line phase shifters.

For a 45° phase shift (Fig. 15), we can see that, for the two versions, the up-state is more important than the down-state dispersion. Fortunately, we have demonstrated previously that down-state capacitance dispersion is higher.

In sub-section 4.1, we had chosen to use average dispersion in first comparisons, i.e. $C_p/C_{p(\text{REF})} = C_p/C_{p(\text{REF})_{\text{up}}} = C_p/C_{p(\text{REF})_{\text{down}}}$.

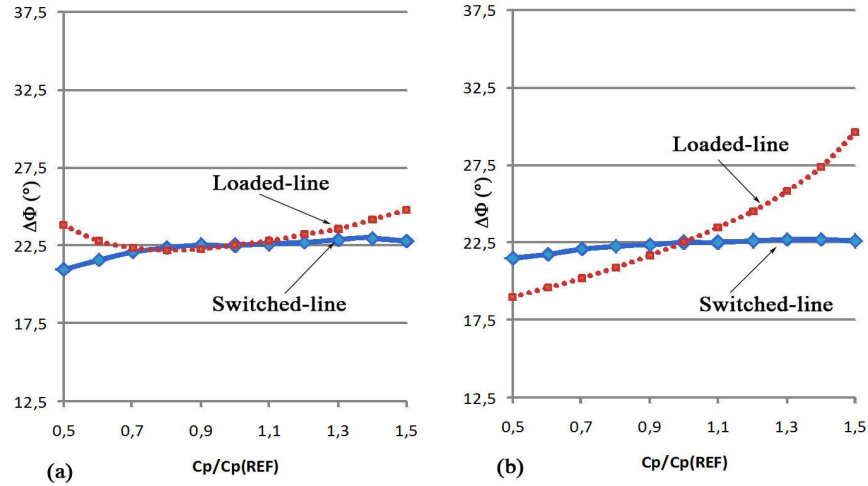


Fig. 16. Average (a) and worst case (b) dispersions for 22.5° switched-line and loaded-line phase shifters.

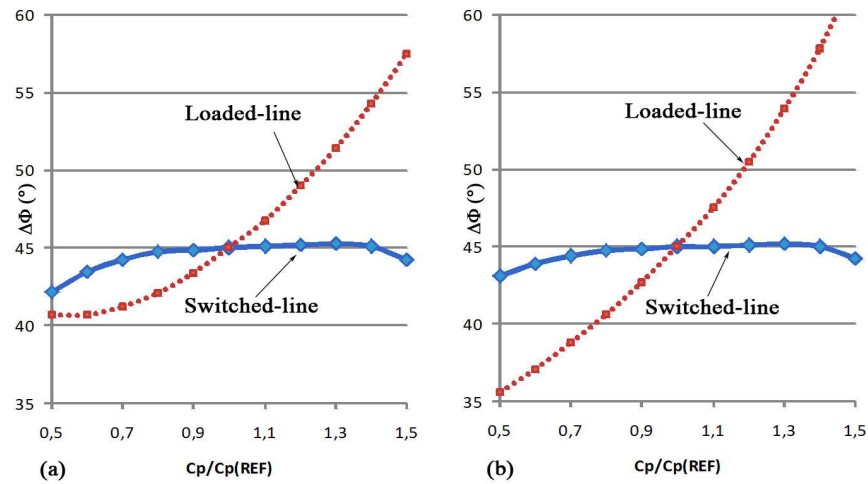


Fig. 17. Average (a) and worst case (b) dispersions for 45° switched-line and loaded-line phase shifters.

Nevertheless, it's interesting to study the worst case i.e. $C_p/C_{p(\text{REF})} = C_p/C_{p(\text{REF})_{\text{up}}}$ and $C_p/C_{p(\text{REF})_{\text{down}}} = 2 - C_p/C_{p(\text{REF})_{\text{up}}}$. In this case, we get the same results as of

the first comparisons but capacitance fluctuations are amplified (Figs. 16 and 17). Indeed, for the loaded-line version, the maximum phase shift deviation may reach up to 17.7° . Consequently, the switched-line version stays the best version for large phase shifts.

N.B.: The circuits are under fabrication. The measured performance will be presented in a following paper.

5. Conclusions

This paper has presented the design of 20 GHz RF-MEMS phase shifters. On the one hand, switch capacitance dispersions in up-state and down-state have been described. On the other hand, we have shown which architecture to choose to get phase shifters that are insensitive to variation of the MEMS capacitances. These results allow to consider the realization of 2-bit phase shifters which will be integrated in microsystems for new phased array antennas.

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