

# A Compact Analytical Modelling of the Electrical Characteristics of Submicron Channel MOSFETs

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**Abstract.** An accurate analytical model for the electrical characteristics of submicron MOS transistors is presented. Original parameters are proposed for the description of the velocity saturation effect. New equations for the electrical transfer characteristics and transconductance are obtained. A theory - experiment comparison is used in order to prove the accuracy of the model. A very good agreement between the transfer characteristics and transconductance measured on the short channel pMOS and the calculated curves based on the model, for different transistor geometries.

## 1. Introduction

The continuing drive to shrink device geometries in all CMOS processes has resulted in devices so small that various high-field effects, such as carrier velocity saturation, become prominent even at moderate voltage [1]–[7].

This paper proposes an comprehensive model of the submicron MOS transistors which takes into account the carrier saturation velocity. Analytical equations are derived for the drain current dependence on gate and drain voltage and for the transconductance in strong inversion.

Transconductance is the most important dynamic parameter of MOS for analogue applications because it reflects the transfer efficiency from input to output. The model is required in order to predict the performance of analogue integrated circuits with a certain degree of precision, prior to fabrication. Some parameters are introduced, for the first time, to illustrate the effect of velocity saturation on the drain current and transconductance. New equations for the drain current and gate overdrive voltage,

meant to define the transition between weak inversion and strong inversion, are also proposed.

The transfer characteristic and the conductance dependence on biasing, calculated using the new model are confirmed by experimental data measured on submicron  $p$ -type transistors produced in 0.35  $\mu\text{m}$  CMOS standard process.

The influence of the geometry factor and of the longitudinal area of the channel on the electrical MOS performance is also investigated.

## 2. Velocity saturation

As technology advances, the feature sizes of MOS transistors are reduced continuously to increase the packaging density of VLSI circuits.

CMOS processes are characterized by the minimum allowed channel length (e.g. in a 0.13  $\mu\text{m}$  technology,  $L_{min} = 0.13 \mu\text{m}$ ). The trend is to reduce  $L_{min}$  in order to increase the transistor density, as well as to operate at higher speeds or, in analogue terms, over a wider bandwidth. The gate oxide thickness decreases and, as a consequence, the oxide capacitance ( $C_{ox}$ ) increases as an effect of scaling. Despite the variation of the surface mobility ( $\mu$ ), the current parameter,  $k = \mu C_{ox}$ , has been steadily increasing because of scaling. Hence, modern submicron devices achieve higher transconductance at the same overdrive voltage ( $V_{OV} = V_{GS} - V_T$ ).

The threshold voltage ( $V_T$ ) decreases with  $L_{min}$ , but the reduction has not been as large as that of the power supply (which was reduced dramatically from 5 V, for the 1  $\mu\text{m}$  CMOS technology, to about 1.8 V, for the 0.35  $\mu\text{m}$  process). As a result MOS devices will operate at low  $V_{OV}$ , which has some drawbacks [2]–[4].

The most important short-channel effect in MOS transistors stems from the saturation of the carrier velocity in the channel. For submicron channels, the model with constant mobility is no longer valid. Mobility is a measure of the velocity acquired by the carrier as a result of the electric field. At low longitudinal electrical fields,  $\xi$  (when the drain voltage,  $V_{DS}$ , is small and/or  $L$  is large), the carrier velocity,  $v$ , increases linearly with the increase of the field and the slope is the surface mobility ( $\mu$ ). At high electrical fields, this slope decreases with the increase of the field, and the velocity reaches a maximum or saturation value, called the scattering-limited velocity,  $v_{scl}$ .

A first order analytical approximation of the dependence of velocity as a function of electric field is given by [2][5][8][9]:

$$v = \frac{\mu\xi}{(1 + (\xi/\xi_c)^\alpha)^{1/\alpha}}, \quad (1)$$

where  $\xi_c$  is the critical field, defined as  $\xi_c = v_{scl}/\mu$ .  $\xi_c$  has a value of 1 V/ $\mu\text{m}$  (1 kV/cm) for electrons and 3 V/ $\mu\text{m}$  (3 kV/cm) for holes in silicon [5][9]. Hence, in an  $n\text{MOS}$  device with  $L_{min} = 0.5 \mu\text{m}$  a voltage drop of only 0.5 V along the channel is needed to produce an average electric field equal to the critical field. For holes, at 300 K,  $\alpha = 1$  as verified in [8][9] and  $\alpha = 2$  for  $n\text{MOS}$  devices [5][9].

### 3. Electrical characteristic modelling

To accommodate velocity saturation begin with the general equation for the drain current in strong inversion [2][3]:

$$I_D = W \int_0^{x_c} qn(x)v_{sc}dx = Wv|Q|, \quad (2)$$

where  $Q$  is the induced charge in the channel and  $W$  is the channel width. At a distance  $y$  along the channel, the voltage with respect to the source is  $V_{cS}$  and the gate-to-channel voltage at that point is  $V_{GS} - V_{cS}$ . We assume that this voltage exceeds the threshold voltage  $V_T$ . Thus the induced electron charge per unit area in the channel is [2]–[4]:

$$|Q|(y) = C_{ox}(V_{GS} - V_T - V_{cS}(y)). \quad (3)$$

The electric field in the channel is

$$\xi = \frac{dV_{cS}}{dy}, \quad (4)$$

where  $dV_{cS}$  is the incremental voltage drop along the length of channel  $dy$  at a distance  $y$  from the source. Substituting (1), (3) and (4) in (2) gives:

$$I_D = W[C_{ox}(V_{GS} - V_T - V_{cS}(y))] \frac{\mu \frac{dV_{cS}}{dy}}{\left[1 + \left(\frac{dV_{cS}}{dy} / \xi_c\right)^\alpha\right]^{1/\alpha}}. \quad (5)$$

In order to obtain an analytical expression of the drain current, we assume  $\alpha = 1$  ( $p$ MOS device).

Separating the variables and integrating along the whole length of the channel gives:

$$\int_0^L I_D dy = \int_0^{v_{DS}} Wk'[V_{OV} - V_{cS}] dV_{cS} - \int_0^{v_{DS}} i_D \frac{dV_{cS}}{\xi_c}. \quad (6)$$

Carrying out these integrations we obtain:

$$I_D = \frac{1}{1 + \frac{V_{DS}}{L\xi_c}} \frac{W}{L} k' \left[ V_{OV}V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (7)$$

Equation (7) is valid in strong inversion for the triode operating region. In the active (saturation) region the current should be approximately independent of  $V_{DS}$ , because the channel length modulation is not included here. Therefore, the boundary

between the triode region and the active region,  $V_{DS,act}$  is the value of  $V_{DS}$  that sets  $\frac{dI_D}{dV_{DS}} = 0$ . By differentiating in (7) we obtained [10][11]:

$$V_{DS,act}^2 = \frac{V_{GS} - V_T}{\frac{1}{V_{DS,act}} + \frac{1}{2V_{OV,K}}} \quad (8)$$

or, after rearranging,

$$V_{DS,act} = \frac{V_{OV}}{\frac{1}{2} \left( \sqrt{1 + 2(V_{OV}/V_{OV,K})} + 1 \right)}, \quad (9)$$

where  $V_{OV,K} = L\xi_c$ , called the knee overdrive voltage, is defined as the overdrive voltage at which the carrier velocity saturation effect becomes significant.

To find the drain current in the active region with velocity saturation, substitute eq. (9) for  $V_{DS}$  in (7). The result is:

$$I_D = \frac{1}{2} \frac{W}{L} k' V_{DS,act}^2. \quad (10)$$

When  $V_{OV} \ll V_{OV,K}$ , the saturation velocity effect is negligible and, from (9) and (10), results:

$$I_D \cong \frac{W}{L} k' (V_{GS} - V_T)^2, \quad (11)$$

$$V_{DS,act} \cong V_{OV} = V_{GS} - V_T. \quad (12)$$

Therefore, the well-known square law dependence of  $I_D$  versus  $V_{GS}$  is achieved. Equations (10) and (11) present the same  $I_D$  dependence, but taking into account that  $V_{DS,act} < V_{OV}$ , results that the  $I_D$  predicted by the classical expression (11) overestimates the current that really flows in the channel. This overestimation occurs even in micron size channels and it is due to velocity saturation.

To further illustrate this behavior, a measured MOS transfer characteristics is plotted in Fig. 1 on two different scales. This curve is compared to the calculated data based on the classical model (eq. (11)) and the new model (eq. (10)). A very good agreement of the new model with the experimental data is obtained.  $I_D$  predicted by the classical expression clearly overestimates the measured current. In the inset graph, we have a zoom of the two models, classical and new. We can see that only for small  $V_{GS}$  the new model defaults to the classical one, just as mentioned earlier.

To examine the limit case when the velocity is completely saturated, let  $V_{OV} \gg V_{OV,K}$ . From (9) and (10) we obtain a directly proportional increase of the drain current with the overdrive voltage:

$$I_D \cong WC_{OX} v_{scl} (V_{GS} - V_T), \quad (13)$$

$$V_{DS,act} \cong \sqrt{2V_{OV}V_{OV,K}}. \quad (14)$$

In strong inversion, the values of  $I_D$  and  $V_{OV}$  are large. For very low currents,  $V_{GS}$  is barely higher and/or can even be slightly smaller than  $V_T$ . This corresponds to the weak inversion operation. The current in active operation is then given by:

$$I_D = \frac{W}{L} k' \frac{2n_s^2 V_{th}^2}{e^2} \exp\left(\frac{V_{GS} - V_T}{n_s V_{th}}\right), \quad (15)$$

where  $n_s$  is the subthreshold slope factor [2]–[5] and  $V_{th}$  is the thermal voltage. The expression clearly shows an exponential dependence of drain current to overdrive voltage, much like the bipolar transistor.

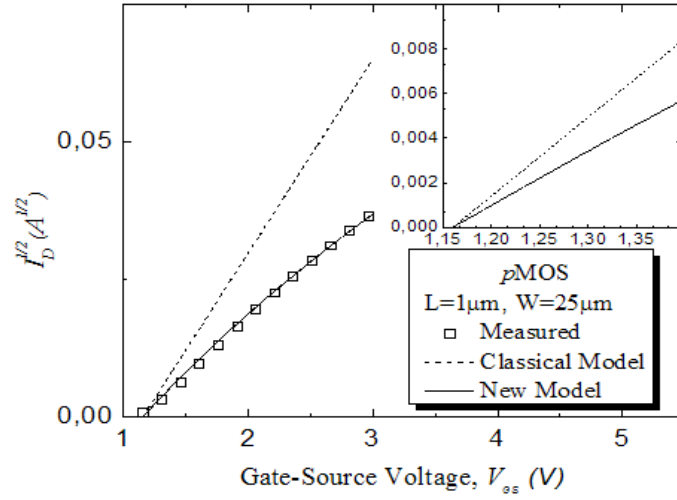


Fig. 1. Square root of  $I_D$  vs. gate voltage.

#### 4. Transconductance modelling

The transconductance,  $g_m$ , the main dynamic parameter of the MOS transistor, can be modified significantly due to the velocity saturation. In strong inversion,  $g_m$  is determined from (9) and (10) by differentiating:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{W}{L} k' \frac{V_{OV}}{\frac{1}{2}(1 + 2V_{OV}/V_{OV,K} + \sqrt{1 + 2V_{OV}/V_{OV,K}})}, \quad (16)$$

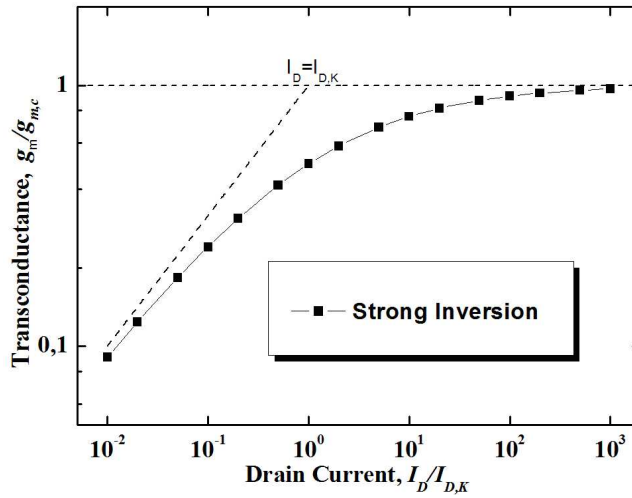
or

$$g_m = \frac{Wk'\xi_c}{1 + \sqrt{I_{D,K}/I_D}} = \frac{g_{m,c}}{1 + \sqrt{I_{D,K}/I_D}}, \quad (17)$$

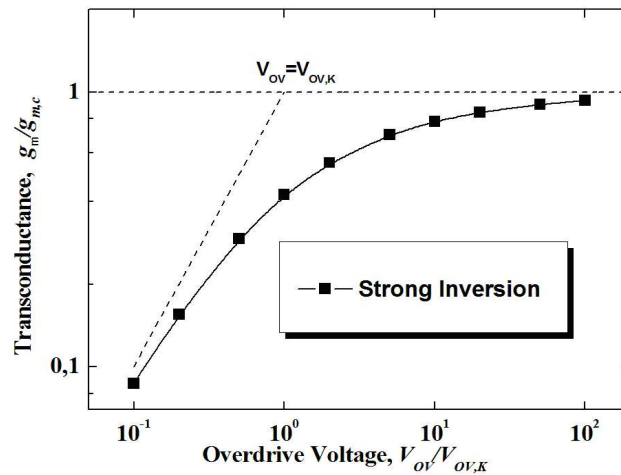
where

$$I_{D,K} = \frac{WL}{2} k' \xi_c^2, \quad (18)$$

$$g_{m,c} = Wk'\xi_c = WC_{OX}v_{scl}. \tag{19}$$



(a)



(b)

**Fig. 2.** MOS transconductance relative to maximum transconductance versus: (a) drain current; (b) overdrive voltage.

$I_{D,K}$  is the knee drain current and  $g_{m,c}$  is the maximum (or saturation) value of the transconductance.

When  $V_{OV} \ll V_{OV,K}$  (which corresponds to  $I_D \ll I_{D,K}$ ) the velocity saturation effect is neglected. In this case, from (11) and (17) results:

$$g_m \cong \frac{W}{L} k' V_{OV} \cong \sqrt{\frac{2I_D}{k'W/L}}. \tag{20}$$

If the carrier velocity is saturated,  $V_{OV} \gg V_{OV,K}$  ( $I_D \gg I_{D,K}$ ), the transconductance reaches maximum value,  $g_{m,c}$ .

Figure 2 plots the  $g_m/g_{m,c}$  ratio as a function of  $V_{OV}/V_{OV,k}$  or  $I_D/I_{D,k}$ , respectively, based on eqs. (16) and (17). Remarkably, we obtain universal curves, valid in strong inversion for any transistor geometry and CMOS process. Each of these curves has two asymptotes, which correspond to the limit cases where the velocity saturation effect is insignificant and dominant, respectively. Extrapolation of these straight lines gives a flexing (knee) point where  $I_D = I_{D,K}$  and  $V_{OV} = V_{OV,K} = L\xi_c$  (Fig. 2) [10].

In weak inversion, the transconductance is:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{W}{L} k' \frac{2n_s V_{th}}{e^2} \exp\left(\frac{V_{OV}}{n_s V_{th}}\right) = \frac{I_D}{n_s V_{th}}. \quad (21)$$

The transition current ( $I_{D,P}$ ) from weak inversion to strong inversion, called the open-channel current, is found by equating the  $g_m/I_D$  ratios calculated with eqs. (10), (17) for strong inversion and (15), (21) for weak inversion, respectively [3]. This yields the following expressions:

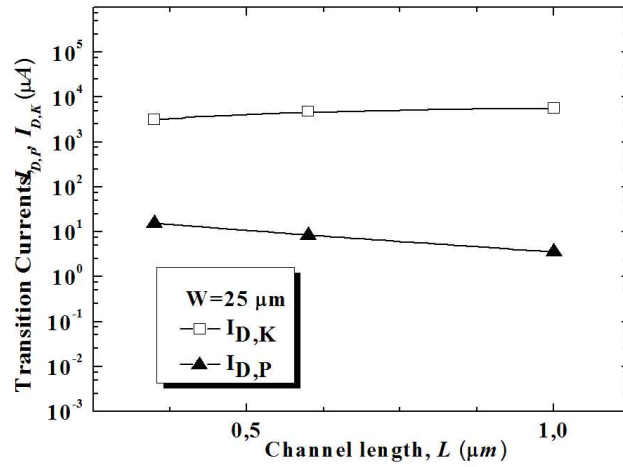
$$I_{D,P} = \frac{W}{L} k' \frac{2n_s^2 V_{th}^2}{\left[\frac{1}{2} \left(\sqrt{1 + 8n_s V_{th}/V_{OV,K}} + 1\right)\right]^2}. \quad (22)$$

To estimate the overdrive voltage required to operate at this current we use expressions (9), (10) and (22):

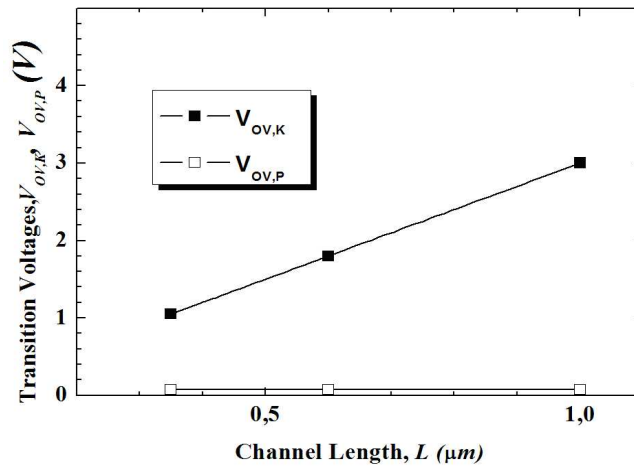
$$V_{OV,P} = \frac{2n_s V_{th}}{\frac{1}{2} \left(\sqrt{1 + \frac{8n_s V_{th}}{V_{OV,K}}} + 1\right)} \left[ 1 + \frac{n_s V_{th}/V_{OV,K}}{\frac{1}{2} \left(\sqrt{1 + \frac{8n_s V_{th}}{V_{OV,K}}} + 1\right)} \right]. \quad (23)$$

If  $V_{OV,K} = L\xi_c \gg 8n_s V_{th}$  the velocity saturation effect is negligible. Eqs. (22) and (23) simplify into the classical equations  $I_{D,P} = \frac{1}{2} \frac{W}{L} k' (2n_s V_{th})^2$  and  $V_{OV,P} = 2n_s V_{th}$ .

The effect of channel length and its associated CMOS technology on the transition drain currents and overdrive voltages is shown in Fig. 3. The difference between  $I_{D,P}$  and  $I_{D,K}$  (and similarly  $V_{OV,P}$  and  $V_{OV,K}$ ) is considerably diminished in submicron devices. Therefore, our model predicts the impact of carrier velocity saturation, at any biasing voltage in strong inversion.



(a)



(b)

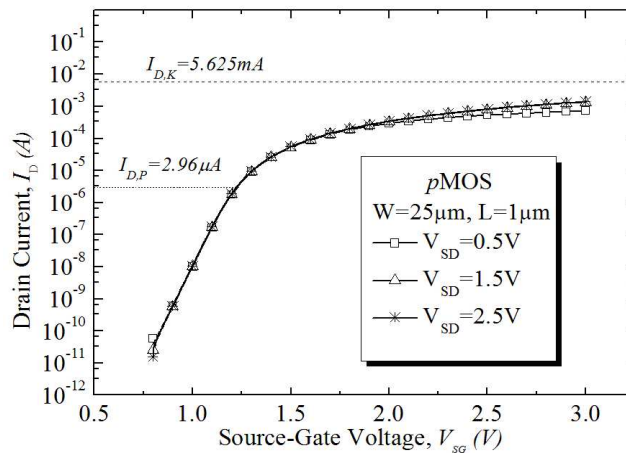
Fig. 3. (a) Transition currents and (b) transition overdrive voltages versus channel length.

## 5. Theory – experiment comparison

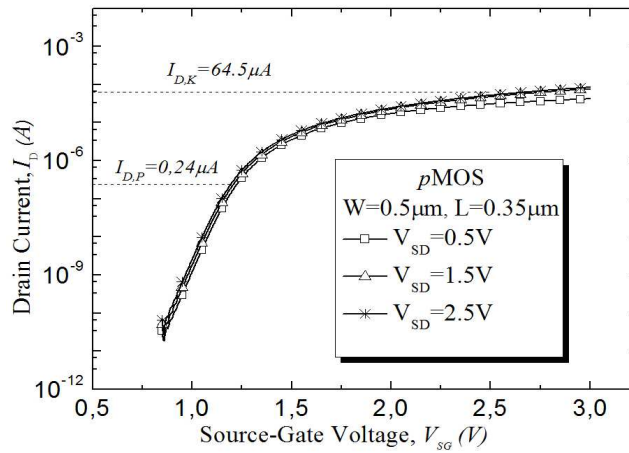
The validation of the model proposed in the previous sections is accomplished by comparison to experimental data measured on  $p$ MOS transistors produced in a standard  $0.35 \mu m$  CMOS process. While this minimum channel size cannot be considered thoroughly deep submicron, it is still true that phenomena that exist in devices with feature sizes smaller than this value are governed by quantum mechanics, rather than by the classical theory. Hence, the MOS capability for analogue applications is di-

minated. However, even in submicron CMOS processes the MOS transistors in a given analogue circuit are deliberately designed to have larger channels for higher performances.

Figure 4 shows the experimental transfer characteristics measured for three values of  $|V_{DS}|$ , for different channel geometries. All the operating regions of the transistors can be observed. In the weak inversion region the drain current increases exponentially with respect to the gate voltage. An obvious overlapping of the characteristics is observed in this region, which proves that the devices operate in the active region ( $|V_{DS}| > V_{DS,act}$ ), at any measured drain voltage. In strong inversion the measured transistors operated in the active region only for drain voltages of 1.5 V and 2.5 V.



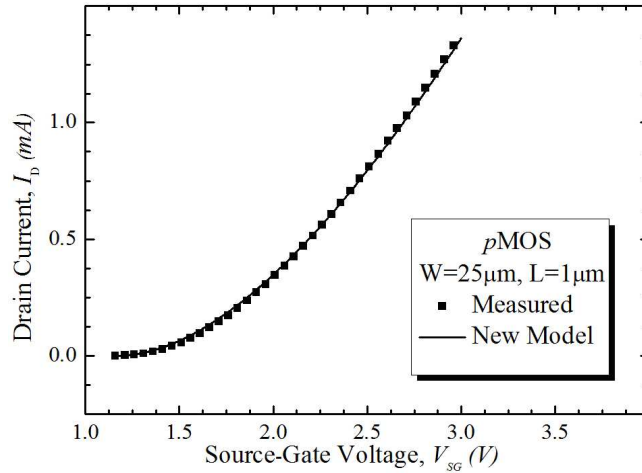
(a)



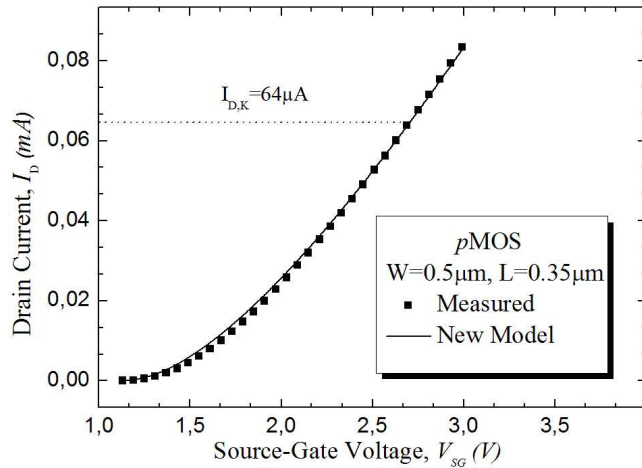
(b)

**Fig. 4.** Transfer characteristics of pMOS fabricated in 0.35 CMOS technology measured at three drain voltages: (a)  $L = 1 \mu\text{m}$ ,  $W = 25 \mu\text{m}$ ; (b)  $L = 0.35 \mu\text{m}$ ,  $W = 0.5 \mu\text{m}$ .

A very good agreement between measured data which correspond to MOS operation in strong inversion and the theoretical curve based on eqs. (9) and (10) can be observed in Fig. 5. Parameters  $V_T$ ,  $k'$  and  $n_s$  used in these equations are given in Table 1.



(a)



(b)

**Fig. 5.** Theory – experiment comparison of transfer characteristics in strong inversion: (a)  $L = 1 \mu\text{m}$ ,  $W = 25 \mu\text{m}$ ;  
(b)  $L = 0.35 \mu\text{m}$ ,  $W = 0.5 \mu\text{m}$ .

The threshold voltage was extracted by the classical technique using the inset graph from Fig. 1. For low  $V_{GS}$  ( $< 1$  V) the square root of the drain current linearly increases with the gate voltage, having the same slope for the classical and new model. The fitting of the experimental data with the theoretical curve was done for the value of  $V_T$  indicated in Table 1.

The current factor,  $k'$ , was obtained by comparing the transfer characteristics measured on  $p$ MOS in strong inversion with the theoretical curve, given by (9) and (10).

The subthreshold slope factor,  $n_s$ , was extracted by fitting the experimental data corresponding to the weak inversion (Fig. 4) with the theoretical curves based on eq. (15).

In Table 1 are also given transition currents and voltages values calculated based on (18), (22), (23). These transition currents are inserted in Figs. 4 and 5.

The open-channel drain current calculated with eq. (22) accurately shows the end of the exponential dependence of the drain current (weak inversion, eq. 15) (see Fig. 4). The knee current indicates the flexing point in the current variation which is due to the velocity saturation effect.

It is interesting to note that the drain current measured on the 1  $\mu\text{m}$  channel  $p$ MOS (Fig. 4a) does not reach the knee drain current calculated with (18). This is explained by the fact that even for the maximum  $V_{DS}$  (2.5 V) the longitudinal electric field is smaller than the critical field (3 V/ $\mu\text{m}$ ). Still, the velocity saturation effect has a considerable influence on this transistor's operation.

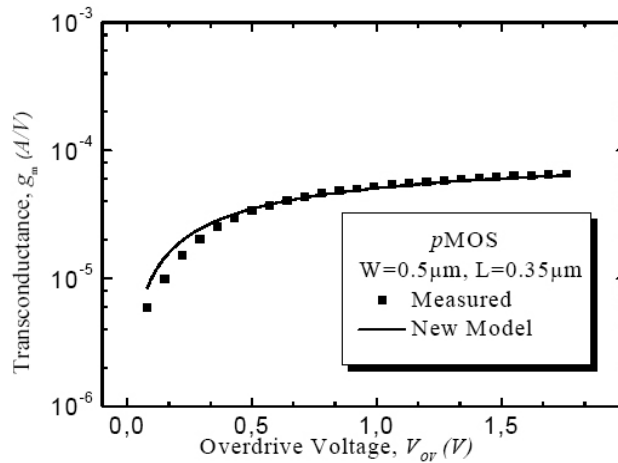
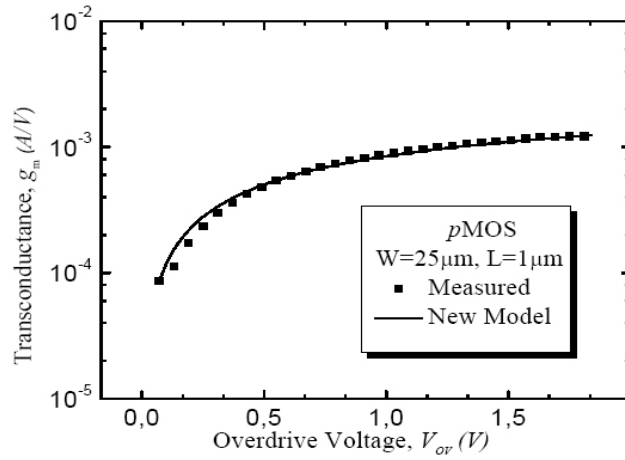
**Table 1.** Extracted transistor parameters

Parameter	CMOS Process	
	pMOS	
L ( $\mu\text{m}$ )	1	0.35
W ( $\mu\text{m}$ )	25	0.5
$V_T$ (V)	-1.16	-1.13
$V_{OV,K}$ (V)	-3	-1.05
$V_{OV,P}$ (mV)	-71.12	-70.24
$I_{D,P}$ ( $\mu\text{A}$ )	-2.96	-0.24
$I_{D,K}$ ( $\mu\text{A}$ )	-5625	-64.6
$n_s$	1.36	1.32
$k'$ ( $\mu\text{A}/\text{V}^2$ )	50	82

Thus, we observe in Fig. 1 a significant difference between the same data (measured on 1  $\mu\text{m}$  channel  $p$ MOS) and the theoretical curve based on the model which ignores the saturation of carrier velocity.

The scaling of the transistor has a considerable effect on the transition currents values and also on the  $I_{D,K}/I_{D,P}$  ratio [10][11]. The currents are dramatically reduced for lower longitudinal area ( $W \times L$ ). Moreover, the current ratio decreases with about one order of magnitude through the reduction of  $W \times L$  from  $25 \times 1 \mu\text{m}^2$  to  $0.5 \times 0.35 \mu\text{m}^2$ . This reduction of the current ratio confirms that the velocity saturation effect matters in the whole strong inversion region for submicron MOS.

The transconductance curves calculated using (16) are compared with the experimental data in Fig. 6. The same good theory – experiment agreement as for the transfer characteristics (Fig. 5) is obtained.



**Fig. 6.** Experimental and calculated transconductance vs. overdrive voltage (absolute value) for: (a)  $L = 1 \mu\text{m}$ ,  $W = 25 \mu\text{m}$ ; (b)  $L = 0.35 \mu\text{m}$ ,  $W = 0.5 \mu\text{m}$ .

## 6. Conclusions

An analytical model of the submicron MOS transistor, which takes into account the carrier velocity saturation in the channel, was proposed. Better expressions for the drain current and drain voltage were deduced. Several new parameters were introduced to describe the velocity saturation ( $I_{D,K}$  and  $V_{OV,K}$ ) and the transition between weak and strong inversion ( $I_{D,P}$  and  $V_{OV,P}$ ). For each of these parameters new analytical expressions were provided for the first time.

The accuracy of the proposed model is proven by comparing it with the experimental data measured on *p*MOS transistors fabricated in the standard 0.35  $\mu\text{m}$  CMOS process. A very good theory-experiment agreement has been obtained for the transfer characteristics and the transconductance. It has been demonstrated that the model correctly predicts a significant effect of the carrier velocity saturation over several analogue parameters of MOS transistor. Calculated values of the parameters ( $I_{D,K}$ ,  $V_{OV,K}$ ,  $I_{D,P}$  and  $V_{OV,P}$ ) using the new expressions were confirmed by experimental data.

A decrease in the knee current to the open-channel current was also observed for submicron devices. Therefore, for these transistor geometries, the saturation carrier velocity is important at any biasing in strong inversion.

The proposed model, being based on just a few parameters, can be easily implemented in an analogue ICs simulator.

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