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Technological aspects and simulation results for the Nothing On Insulator device developed into a planar technology

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Abstract. This paper presents the simulations results of a planar variant of Nothing On Insulator device starting from Si-surface preparation till the fine oxide configuration of few nanometers. A dry oxidation at lower temperature is a better process to a higher temperature in a time under 1min. But the final experimental technological tests find the best solution - relatively high temperature, acceptable time of 5-8 min, but dilution of the O2 fluids in the furnace adding N2 in a suitable ratio.

The functionality of the planar variant p-NOI was tested by Atlas simulations in two cases: (i) a p-NOI structure with 10nm SiO2 when it is compared to a standard simulated MOSFET from Atlas and (ii) a p-NOI structure with SiO2/HfO2 stack when it is compared with an insulator stack with similar composition of one of the lasts generation fabricated MOSFET. The conduction mechanism obeys to the Fowler-Nordheim's law. The current flow from source to drain occurs in absence of an inversion channel. A similar investigated device by other authors is a fabricated MIM (Metal-Insulator-Metal) structure, which is compared with the actual p-NOI simulation. The simulations fit over the experimental picked points from different resources.

Key-words: Tunneling device, nanoelectronics, simulations, technological steps.

1. Introduction

Novel devices are recently proposed: Tunnel-FET, SOI for CMOS sub10nm or NOI (Nothing On Insulator) transistor, [1-4]. A NASA research group fabricated in 2012 a tunneling transistor with vacuum channel, with closer operation voltages to previous MOSFET generations [5, 6].

In the context of this class of tunneling devices, the NOI (Nothing On Insulator) device was theoretically described in 2005 [7], and was investigated by simulations in the last ten years [8]. The main difficulty in the NOI transistor manufacturing consists in the width of the vacuum as a cavity of 2nm between Source and Drain islands, [9]. This paper proposes a planar NOI variant (p-NOI), changing the vacuum tunneling by the oxide tunneling, [10]. Rotating the NOI structure the width problem becomes the thickness problem, fig. 1. The oxide configuration of 2....20nm thickness on a Si-wafer can be processed in any Si-technology. The Source is upper placed and the Drain can be the bottom contact. The benefit of the exponential ID-VD dependence can be kept, using the oxide tunneling, instead the vacuum tunneling, because the same Fowler-Nordheim formalism is anyway fulfilled, [11]. The first experimental arguments of the tunneling current in sub-30nm gate insulator are demonstrated by the measured gate currents in the last MOSFET generations, [12], as main argument to introduce the p-NOI device.

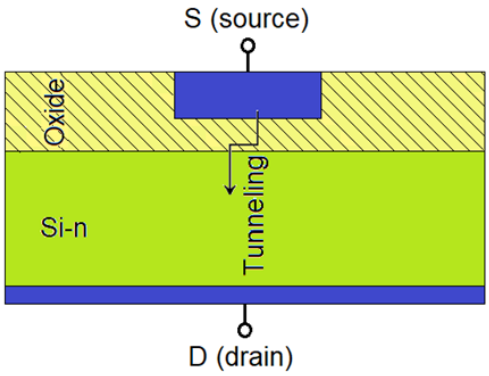

Fig. 1. The work principle of the p-NOI variant: the tunneling current flows on vertical direction.

The first target of this paper is to present a technological flow and to test the p-NOI functionality. Some technological steps during the device preparations indicate the optimum solution to grow ultra-thin oxides on a Si-wafer.

2. Simulations of technological processes

The longitudinal source-drain tunneling current inside a NOI transistor, now occurs on the vertical direction in planar p-NOI, between Drain to Source, Fig. 1. At this stage, the p-NOI structure seems to be a MOS capacitor if the Source terminal is replaced by the Gate terminal. But, for p-NOI, the Source contact is top placed, onto the SiO2 layer, while the drain electrode in direct contact with Si-region can be placed on the substrate or can be laterally raised on the wafer surface.

The Athena from Silvaco software is used to simulate the technological flow. The start wafer is Si, $< 100 >$, n-type with phosphorus doping of 10^{15}cm^{-3}, fig. 2a. To avoid Schottky contacts, the wafer is pre-diffused at 1000°C, 60 min., up to 10^{20}cm^{-3} Phosphorus concentration at surface, fig. 2b. Then the wafer is covered by 2nm oxide, by dry oxidation and HCl atmosphere for 5min at 625°C, Fig. 2c. If it is aimed to grow an oxide of 10nm, keeping the oxidation time of 8min, the annealing temperature can be raised to 880°C.

Then, the Source is laterally configured. For instance, Polysilicon of 20nm thickness is deposited above oxide. After right etching of the polysilicon, results the configured Source of the p-NOI structure. Then the oxide is right etched, fig. 2d. The Aluminum layer is deposited onto the entire wafer. During the next mask, the metal is etched off in the left side, to define the Drain contact. The final technological version of the p-NOI variant is available in fig. 3. A zoomed view around the oxide film 2nm is presented.

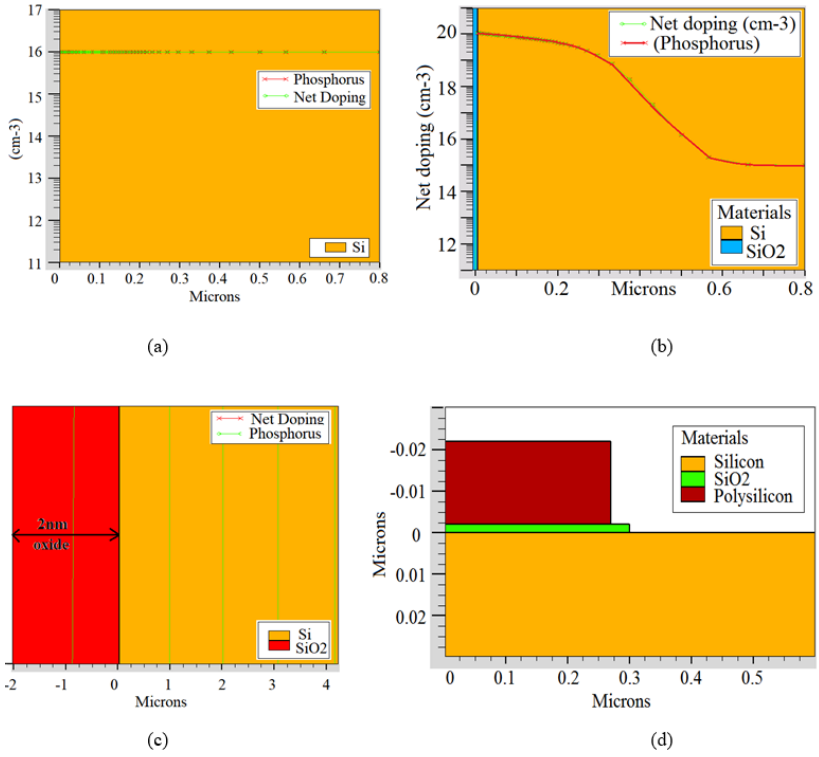

Fig. 2. (a) The Start wafer; (b) the prediffused n+-layer; (c) after oxide removal, then a clean oxide is grown in dry O2, 1atm HCl 3, 625°C, for 2nm oxide on wafer; (d) Drain metal configuration.

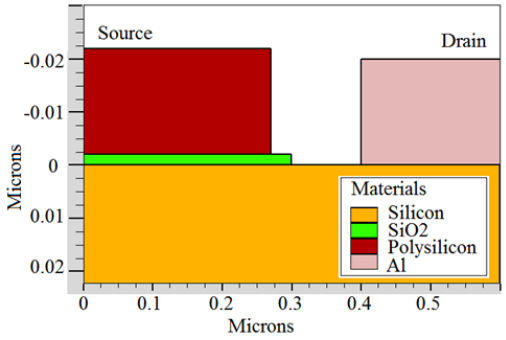

Fig. 3. The Athena final results during the technological flow of the p-NOI device in a complete round, including Al-Drain lateral configuration.

The p-NOI gets now clear distinctive elements against MOSFET, like lateral Drain contact on a n+ film - the same n+ film used under the Gate oxide, Fig. 3.

3. Technological steps during the fabrication process

The fabrication of the p-NOI planar variant was preceded by the masks design. In this way, a top view on the p-NOI structure is available in fig. 4.

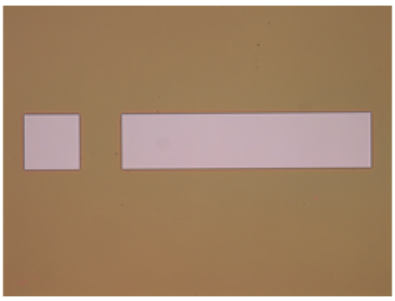

Fig. 4. The configuration of Source and the Drain as lateral electrode with larger surface.

Accordingly to the data from the previous simulation stages, we proposed the next technological flow for the realization of the p-NOI structure, in planar technology:

- start Si wafers CZ, orientation $< 100 >$, type-n, resistivity of 5-8 cm,
- additional phosphorus doping by diffusion at the surface, with a high concentration of 10^{20}cm^{-3},
- during the diffusion of impurities, simultaneously a silicon dioxide (SiO2) layer is grown, reaching 330nm thickness. This layer of SiO2 was used for next photolithographic technique,
- windows (170 x 850μm) were opened for the growth of thin SiO2 - MASK-1,
- an oxide of 3,6nm was grown, at T=800°C, with dry oxidation, in 5 min, in O_2: N_2 (1:1) gases,
- follows an annealing for 20min in N_2/ output 5 min in N_2,
- deposition by sputtering, Cr:Au (20:200)nm for the Drain configuration, instead Polysilicon electrode,
- finally, source/drain electrodes are configured by lift-off.

Few deviations are applied versus the simulations. The main oxidation process is better to be at a higher temperature; therefore the temperature was increased to 800°C instead 625°C, changing the fluids inside the furnance: O2: N2 instead high concentration of O2. In this way, the oxide grows slower, cleaner and sharper.

Another changing concern the selection of the source/drain metal composition: Cr:Au metals to ensure different materials as contacting layers, instead of Al or Polysi. Chromium ensures a better gold adherence.

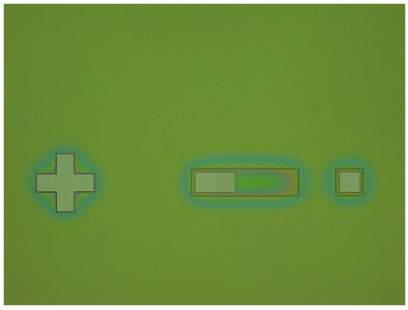

Fig. 5. The final p-NOI structure at optical microscope.

4. Validations by simulations of the p-NOI device functionality

In order to compare a p-NOI device with a NOI device, a 2nm oxide thickness would be necessary, as the 2nm gap of the NOI transistor. But, these simulated comparisons were performed elsewhere [13]. Now, a p-NOI variant with an average oxide thickness of 10nm is considered, because some experimental similar structures, like Metal-Insulator-Metal (MIM) [14] or gate MOS oxide [15] were considered in this range. The p-NOI structure is close to a MOS capacitor, with lateral source contacts on the n^+-type semiconductor, raised onto the surface, both in the left and right parts of the Drain on oxide region, fig. 6. Consequently, the simulations can be easily compared to similar MOS capacitors from MOSFETs.

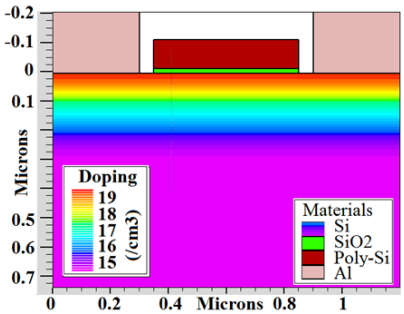

Fig. 6. The simulated structures of p-NOI device variant with 10nm oxide, similar to a MOS transistors.

The 10nm oxide thickness for p-NOI device, allows similar tunneling current as in a standard simulated MOSFET structure from the Silvaco examples [15], which also possesses 10nm gate oxide. This MOSFET configuration presented by Silvaco as a standard example, benefits on a best fitting of the simulated static characteristics to the experimental characteristics. Both devices

have the Si-substrate with doping profiles as in Fig. 6, SiO_2 insulator of 10nm thickness, upper source contact and lateral drain contact.

Both standard MOSFET [15], experimental MIM [14] and p-NOI device with 10nm SiO2, corresponding to fig. 6, are contacted to V_{Sb}=V_S=0V, while V_D increases from 0V to 30V. The main tunneling mechanism for the gate current of the MOSFET or Drain current of the p-NOI is Fowler-Nordheim model, activated by the FNORD parameter in the model statement, both for the standard MOSFET and p-NOI device, Fig. 7a. The p-NOI device has a length L=0.5μm measured under the oxide from Fig. 6, while the width on Oz axis is W=1μm, as the default value admitted in 2-D Atlas simulations.

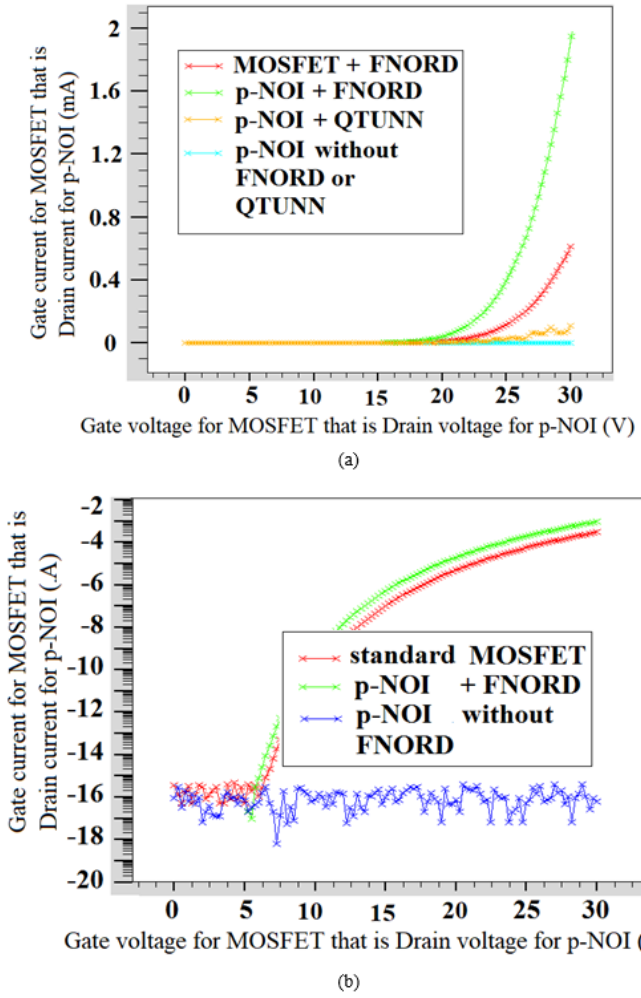

Fig. 7. The I-V curves for MOS and p-NOI with different models at: (a) linear scale; (b) log scale.

An alternative phenomenon that can lead to a gate current increasing is the direct quantum tunneling. This event occurs if the oxide is thin enough to create a quasi-rectangular barrier potential between the gate electrode and semiconductor in MOSFET. Subsequently, the drain cur-

rent of p-NOI device is simulated by QTUNN parameter in Fig.7a. But the simulations prove an insignificant quantum tunnelling components, 20 times lower than FNORD component. Hence, in next simulations QTUNN parameter is ignored. The Fowler-Nordheim mechanism offers the maximum current excursion till 2mA for p-NOI with donor doping of 10^{19}cm^{-3} under the gate oxide and till 0.6mA for MOSFET with acceptor doping of 10^{17}cm^{-3} under the gate oxide.

Fig. 7b comparatively presents the I-V characteristics of the standard MOSFET and 10nm-p-NOI at logarithmic scale for: (i) p-NOI without FNORD parameter; (ii) p-NOI with FNORD model; (iii) standard MOSFET with FNORD model. If FNORD parameter is absent, a noisy almost-null current is captured through p-NOI structure, Fig. 7b.

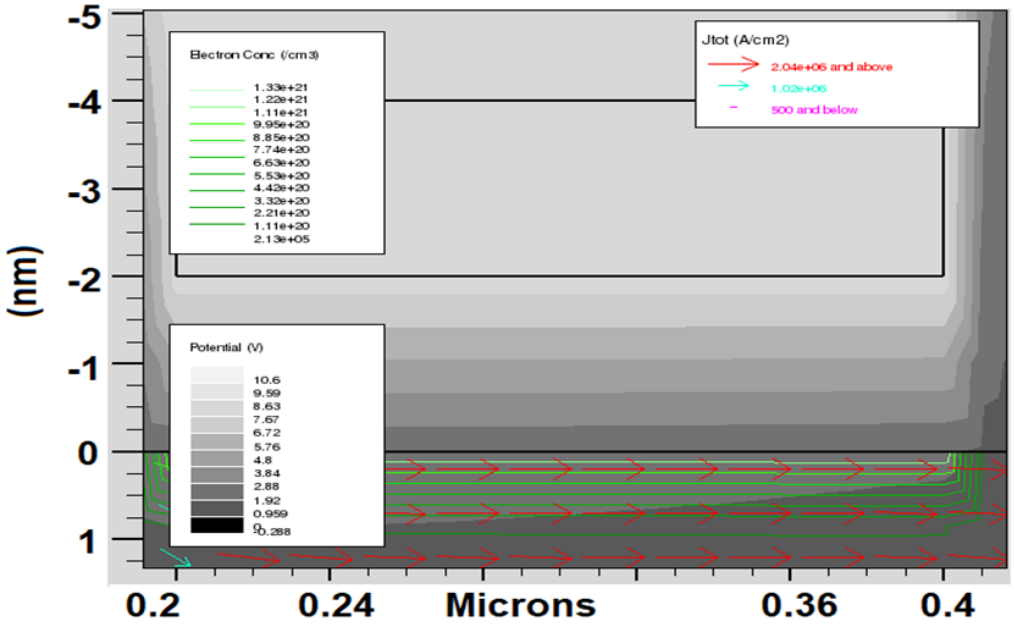

Fig. 8. The current vectors flow validation through the p-NOI device at V_D=10V and V_S=0V.

In the case of p-NOI structure, the current flow starts from the drain and laterally occurs toward source electrode that is grounded, Fig. 8. This is possible for the p-NOI structure, which includes a MOS capacitor working in accumulation, so that the conduction occurs by an electron n-type film.

5. Comparisons with experimental picked points for a p-NOI variant with SiO2/HfO2 stack insulator

The previous case with 10nm oxide thickness was selected only to can be compared with the standard MOSFET with 10nm oxide. Considering that the NOI-transistor better works with 2-5nm insulator wide for tunnelling [8], the actual p-NOI structure must be compared with MOSFETs with this order of magnitude for the stack gate insulator. In literature, a MOSFET with sub-10nm stack insulator up to 1.39nm, SiO2/HfO2 type, is depicted, [12]. In p-NOI case, the

mesh gets 4nm on Ox axis and 1 to 200nm on Oy, [16]. This p-NOI structure with 6nm HfO2 over 1nm SiO2 appears in Fig. 9.

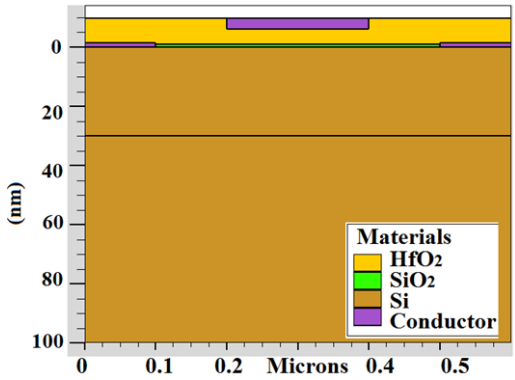

Fig. 9. The p-NOI structure with 6nm HfO2 over 1nm SiO2.

Fig. 10 presents the current vectors density inside this p-NOI structure with HfO_2, polarized at V_G=10V. The total current density has a maximum of 2.6x10cm^{7}A/cm^2 in n^+-film, near source and drain, after Atlas running, Fig. 10.

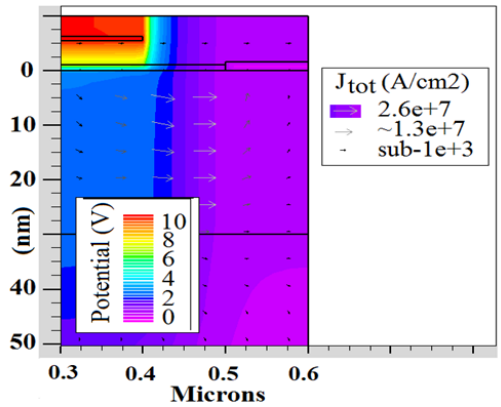

Fig. 10. The potential contours and current vectors through the p-NOI structure with HfO_2 biased at 10V-detail on Ox and Oy.

Fig. 11 makes a comparison between the simulated I-V characteristics thru oxide of p-NOI variants with 1nm-SiO_2/4nm-HfO_2, 1nm-SiO_2/8nm-HfO_2, and sole 1.39nm-SiO_2 besides to some experimental I_G-V_G picked points from a fabricated MOSFET with 1nm-SiO_2/4nm-HfO_2 [12] and some experimental I-V picked points of the Metal-Insulator-Metal nanostructure with 10nm oxide as Insulator, [14]. The shape and current variation are quite similar for p-NOI and experimental MOSFET. For MOSFET the experimental gate current density varies from 10^{-6} to 10^2A/m^2 that is a current variation from 10^{-18} to 10^{-10}A, Fig. 11.

The results are in a good agreement with the literature [12, 14], proving the Fowler-Nordheim tunnelling conduction as the main mechanism inside the p-NOI devices.

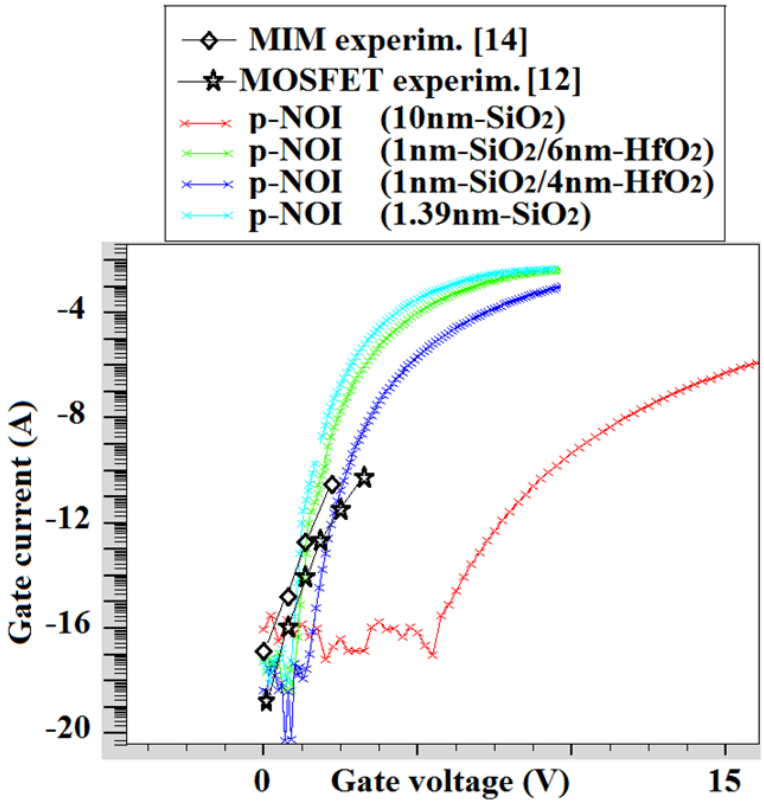

Fig. 11. The experimental I_G-V_G picked points from an experimental MOSFET [12] besides to simulated curves of different p-NOI variants.

Moreover, the comparisons show that p-NOI structure with 1nm SiO2 / 6nm HfO2 or p-NOI with 1.39nm SiO2 provide higher current at least for an operating gate voltage higher than 5V against the MOSFET [12] or MIM [14]. However, to transform a p-NOI simulation into a practical p-NOI with only 1.39nm SiO2 is challenging for the actual technology. On the other hand, in only few years, the MOSFETs will reaches, too these equivalent gate oxides. If the p-NOI simulated superiority will be conserved in practice, very soon they could be used.

The E/4 Si wafer is a n-type $< 100 >$ wafer, which is implanted with Phosphorus to increases the doping concentration to the surface, as n+ layer. To achieve so thin oxide, a thermal oxidation at 800 °C for 5 min in mixed O2: N2 environment, occurs. The ideal target is 6nm, but the real SiO2 thickness can be mapped by ellipsometry, Fig. 12.a. Here we observe variations from 5.586nm up to 6.287nm for the SiO2 thickness. The SiO2 roughness is available in fig. 12.b, after AFM analysis. They reveal higher non-uniformities, as hills and valleys of maximum 3nm height along a 0...10μm square area.

6. Experimental tests

After a technological flow, 6nm oxide is grown onto a Si wafer, code E/4.

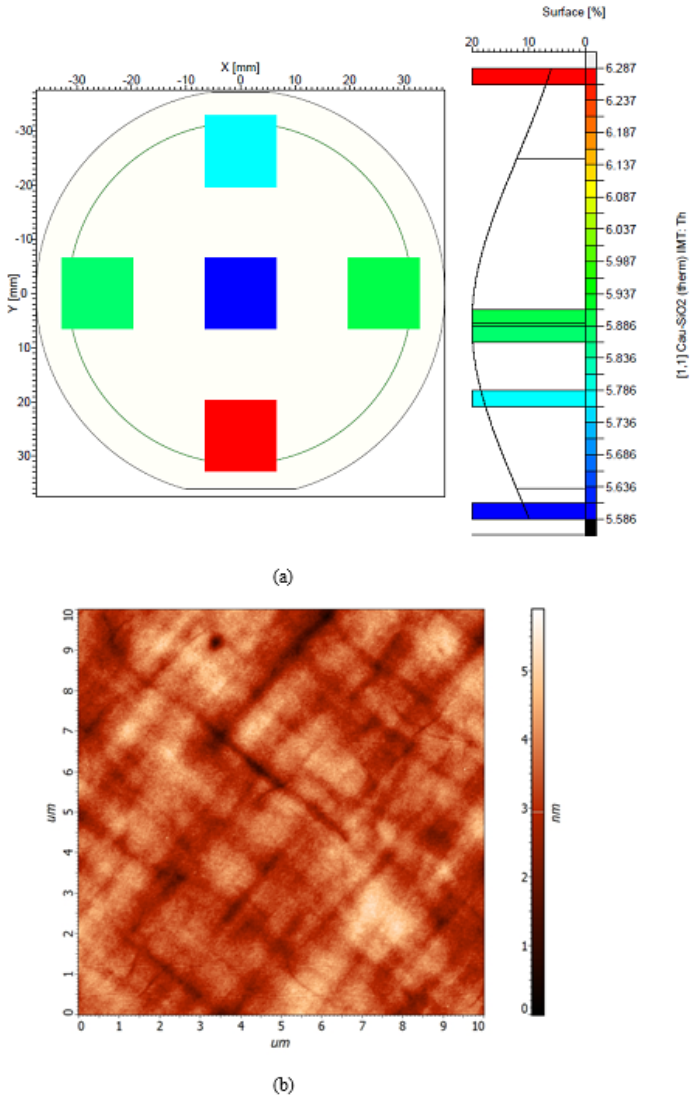

Fig. 12. The characterization of E/4 code wafer with 6nm SiO2: (a) by ellipsometry, (b) by AFM.

The E/4 Si wafer is a n-type $< 100 >$ wafer, which is implanted with Phosphorus to increases the doping concentration to the surface, as n+ layer. To achieve so thin oxide, a thermal oxidation at 800 °C for 5 min in mixed O2: N2 environment, occurs. The ideal target is 6nm, but the real SiO2 thickness can be mapped by ellipsometry, fig. 12.a. Here we observe variations from 5.586nm up to 6.287nm for the SiO2 thickness. The SiO2 roughness is available in fig. 12.b,

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7. Conclusions

In this paper, a technology of the planar variant p-NOI is proposed, starting from some simulations selections till the final masks and proper technological flow. The conclusion was to grow a thin oxide of 2-3nm is better to manipulate the wafers at a realistic time of 5-8min. This implies two ways: either a low oxidation temperature of 625°C, or to keep also a realistic temperature of 800°C but a O2 fluid dilution, mixing N2 gases in the furnace.

From the point of view of the device functioning, the Fowler-Nordheim mechanism was firmly demonstrated to be the main tunnelling current component in this p-NOI device. When the p-NOI structure gets the SiO2/HfO2 insulator stack, as the last generation of MOSFETs, the measured gate current of the transistor fit very well among the simulated points of the p-NOI structure with HfO2.

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