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Ascertaining the root-cause of discrepancies between simulations and measurements for a SC DC-DC converter

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Abstract. This paper presents a methodology for ascertaining the root cause of discrepancies between simulation and measurement results related to particular parameters and/or features of an integrated circuit. The main idea is to assess the sensitivity of the wanted IC parameter/feature to factors which may not have been accurately and comprehensively considered during pre-silicon verification – such as block-level non-idealities, internal parasitic components and inaccuracies in modeling the package and external components. This is achieved by running parametric simulations on amended views of the top-level IC schematic and the main simulation testbench. Behavioral models of large functional blocks within the IC are employed, not only to reduce the simulation time but also to allow for a quick assessment of the impact block-level non-idealities may have on the IC performance. After identifying the factors that impact most the IC parameter/feature under test, the designer can find the sets of values/combinations of some of those factors that yield simulation results most similar to measurements. Finally, the system layout, the simulation testbenches and the measurement setup are analyzed in detail, focusing on possible root cause(s) of the factors/combination of factors indicated by simulations. A real-case deployment of this methodology is presented: a switched-capacitor DC-DC converter, whose measured output voltage ripple had a different shape and larger amplitude than those predicted by simulations. The proposed methodology can be embedded in the design flow, as well, from deriving block-level parameters from general system requirements to setting clear requirements for layout routing of key tracks within the IC.

Key-words: Microelectronics, verification methodology, analog and mixed-signal IC, root-cause identification, Verilog- A model; switched capacitor DC-DC converter; voltage output ripple.

1. Introduction

The development of a new *integrated circuit* (IC) typically encompasses the following steps: setting the requirements/specifications, defining/choosing the system architecture, derivation of block-level specifications, block-level design, top-level pre-silicon verification through simulations, manufacturing and post-silicon verification and characterization through physical measurements and tests. The last step is vital, as it proves whether the resulting IC meets the set requirements or not [1]. Comprehensive pre-silicon simulations, covering all required features and parameters, as well as standard and user-defined test, are essential for ensuring compliance with specifications [2].

However, it is not always possible to run all necessary simulations, especially due to the time and resources required. This is often the case for switched-mode power management circuits, where large jumps in signals value are unavoidable, leading to convergence issues [3]. In addition, noisy lines–such as those corresponding to nodes that swing fully between the supply rails–coexist with noise-sensitive lines, such as voltage references. To assess the impact of switching noise coupling, one must run extensive simulations on detailed views of the entire system, that include parasitic components extracted from the top-level layout of the IC. Such views are available quite late in the design cycle and the corresponding netlists are huge, requiring substantial computational resources to run simulations on.

Moreover, the accuracy of simulation results is limited by model inaccuracies – including the models of external components and IC package – as well as phenomena not considered by standard simulators, such as electro-thermal-mechanical interactions [4], and substrate noise.

All these can lead to important differences between pre-silicon simulations and post-silicon measurement results. This is reflected by the old designer adage: “Silicon measurements often give bad answers to questions the designer has not asked in simulations”. Effective and reliable identification of the root-causes of these differences is essential for re-design. This implies reproducing in simulations the results yielded by measurements. However, the brut-force approach – running complex simulations on top-level views that include post-layout extracted components, called hereafter PEX simulations – is time – and resources-intensive and may not be successful, if the root-cause is related to modeling or simulation limitations.

A more effective approach is presented in this paper. Section II describes a methodology for ascertaining the root-cause of discrepancies between simulation and measurement results, based on behavioral models for large functional blocks within the IC; the models not only reduce the netlist size but also allow the designer to analyze the effect some block-level non-idealities may have over the performance of the entire system [1], [5].

Moreover, key parasitic components can be added to the modeled system, and their effect can be easily assessed through parametric simulations. The proposed methodology is deployed on a real-life case presented in Section 3: a *switched-capacitor DC-DC converter* (SCDC), whose measured output voltage ripple has a different shape and a far larger amplitude than predicted by simulations. Section 4 details the main steps performed to identify the root-cause of these differences. The main points are summarized in the last Section, which also presents the main conclusions than can be drawn from this work.

2. Description of the proposed methodology

Figure 1 presents the flow chart of the proposed methodology for ascertaining the root-cause of simulation-versus-measurement discrepancies related to a particular IC parameter/feature. The main idea is to assess the sensitivity of that feature to factors which may not have been accurately and comprehensively considered during pre-silicon verification.

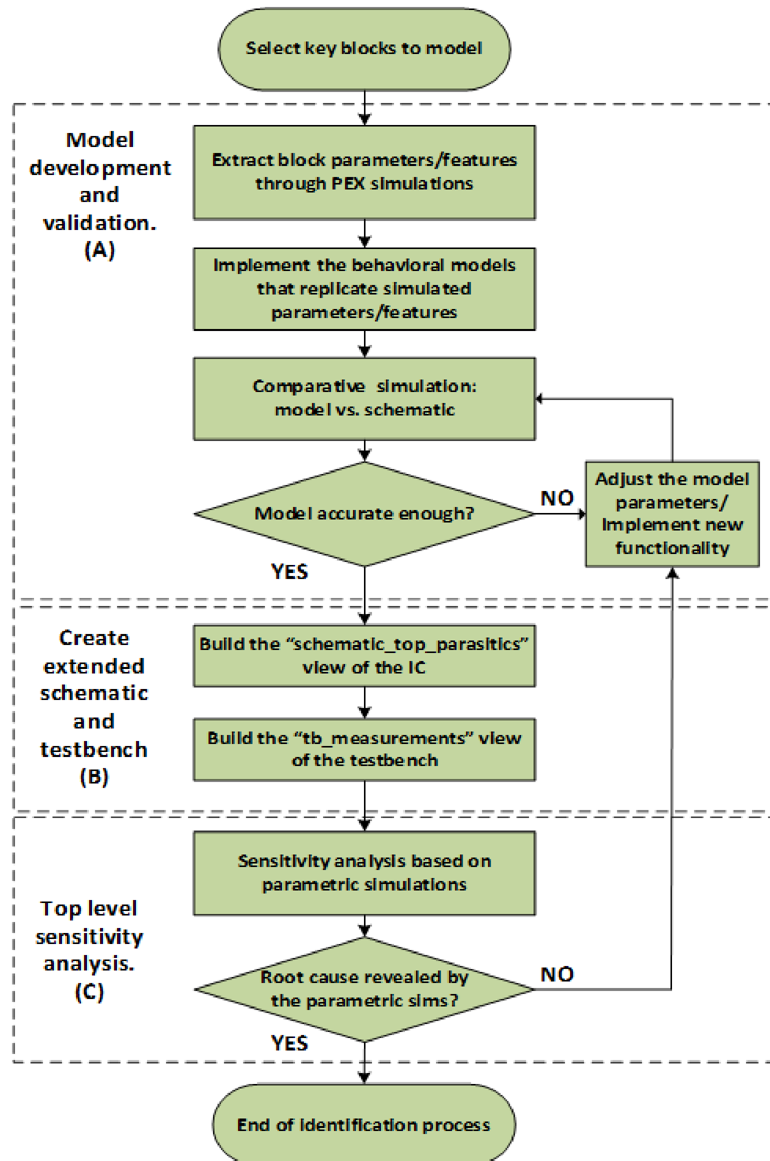

Fig. 1. Flow chart of the proposed methodology for identifying the root cause of discrepancies between simulation and measurement related to particular parameters and/or features of an integrated circuit.

The first step consists of the development and validation of Verilog-A behavioral models for the main functional blocks within the IC. These models should not only yield simulation results as close as necessary to the PEX simulations run of the corresponding block but should also allow for the value of key parameters of that block to be swept over a wide range.

Next, an amended version of the top-level schematic is created by adding the main parasitic components related to sensitive lines, such as voltage references, and noisy lines, such as those corresponding to nodes that swing fully between the supply rails.

The initial values of these parasitics are derived by using PEX tools on the top-level layout. For example, the total parasitic capacitance on a node can be read from a PEX view, then a capacitor with that value is placed in the schematic. Let us call "schematic_top_parasitics" the resulting representation of the IC. Similarly, an amended version of the simulation testbench should be created, to reflect as accurately as possible the measurement setup and include parameters that describe non-idealities of the package and external components. A typical example is the ESR of the load capacitor. Let us call "tb_measurements" the amended testbench, which includes the "schematic_top_parasitics" view of the IC.

The main step consists of running parametric simulations on the amended versions of the top-level schematic and testbench; the values of parasitic components, as well as the values of key parameters defined in the block-level Verilog- A models, are swept iteratively, individually and in groups. These steps are detailed in the following sub-sections.

A. Model development and validation

First, a thorough analysis of the system must be performed, in order to decide which functional blocks should be prioritized for behavioral modeling and which of their features/parameters should be modeled in most detail. Two complementary selection criteria should be considered:

- blocks and features most un-likely to cause the simulations-measurements discrepancies, but whose schematic representations yield large netlists. A typical example is digital control blocks. By using functional models instead of schematic views, one can significantly reduce the simulation time for the ensuing top-level simulations required by the methodology proposed here.

- blocks and features for which even small inaccuracies in schematic simulations can significantly impact the system performance. For example, small errors in modeling the ON resistance of power switches may result in large differences between the simulated and measured values of the voltage drop across them. In the Verilog-A model of such a switch the ON resistance appears as a parameter, which can be swept over a range wide enough to cover possible modeling inaccuracies with a reasonable margin.

A simple yet effective way of validating the behavioral model of a block is to compare the results it yields in simulations with the corresponding results yielded by schematic (and PEX) representations of that block. One should consider the trade-off between accuracy – which implies complex models - and simulation-time effectiveness – which is crucial for the proposed methodology. A solution is to develop the models iteratively, starting with simpler/less accurate models which are refined if, and as required by subsequent steps.

B. The "schematic_top_parasitics" and "tb_measurements" views

Often, it is not practical to run comprehensive simulations on detailed top-level views of the entire system, which include parasitic components extracted from the top-level layout of the IC. Instead, the views described above should be built by adding key parasitic components, such as:

- series resistance of metal lines – especially for lines carrying large currents, but for unbuffered reference voltages, as well.

- capacitances placed between noisy lines – such as the gate of power switches, which swing fully between the supply rails and have intrinsic large capacitances – and noise-sensitive lines such as voltage references and feedback nodes with large impedances.

- series inductances associated with long metal lines and bond wires.

- ESR of external capacitors.

Usually it is difficult to obtain accurate values for these parasitics by using PEX tools, so the plan is to parameterize them, in preparation for subsequent parametric simulations. Again, one should select carefully the parasitics included in the "schematic_top_parasitics" view, as they can impact simulation time.

C. Sensitivity analysis based on parametric simulations performed on the "tb_measurements" and "schematic_top_parasitics"

After completing the two steps described above, the designer can easily assess the system sensitivity to particular block-level non-idealities and parasitics by running parametric simulations. Of course, this analysis should focus on the system parameter/feature for which the discrepancies between simulation and measurement results are the largest/most important. This helps reduce the number of necessary simulations, but the number of parameters to be considered – as well as the combinations between them – can be very large.

Therefore, one needs to devise a strategy to reduce the number of simulations. Here is a suggestion:

- start with the block most unlikely to cause the simulation-versus-measurement discrepancy under analysis. For this, simulations are run on the "schematic_top_parasitics" with only the chosen block represented by its model. Parametric simulations that sweep the value of each block parameter within an appropriately wide range indicate whether that parameter has a strong enough impact on the IC performance to be considered among potential root causes or no.

- if these simulations suggest that a block is indeed not responsible for the simulation-versus-measurement discrepancy, the analysis moves to the next block(s), in increasing order of likeliness to be the culprit. In the ensuing parametric simulations, the block (and subsequently all blocks) checked and found not responsible for the discrepancy can be represented by its/their Verilog- A models. This helps reduce the simulation time.

- once parametric simulations reveal sensitivity to a particular block parameter, a more detailed analysis should be performed in order to establish if that parameter could be the sole cause of the simulation-versus-measurement discrepancy under analysis. If not, the parametric simulations continue for the remaining functional blocks, then for the parasitic components included in the "schematic_top_parasitics" view.

- after assessing the system sensitivity to all block-level non-idealities and parasitics the designer can select the ones that directly impact the system parameter/feature related to the simulation-versus-measurement discrepancy under analysis. Then the analysis focuses on finding combination(s) of these factors that yield simulation results most similar to the measurement results.

- finally, the system schematic and layout are analyzed in detail in order to establish the root cause(s) of the factors/combination of factors indicated by the simulations described above.

3. A real-life example: debugging a switched capacitor DC-DC converter

The methodology presented in the previous Section was used to identify the root cause of discrepancies between pre-silicon simulations and post-silicon measurements related to the output voltage ripple of a *switched-capacitor DC-DC converter* (SCDC) for automotive applications.

Here are the main requirements set out for this converter: fixed output voltage, V_{OUT}=5V, maintained over a large input voltage domain, V_{BAT}=11V to 40V; output voltage ripple smaller than 50mV; maximum load current, ILmax = 200mA, peak efficiency greater than 80%(at ILmax). The SCDC employed two capacitors of equal value, $C_{FLY} = C_L = 1\mu F$ and its switching frequency was set to 500kHz.

The converter was designed in a HV 0.18 μm CMOS technology. All the requirements listed above were met in simulations. Measurements performed on a test chip yielded results acceptably close to simulations except for the output voltage ripple.

The working principle of the SCDC converter is briefly presented in the following Subsection, then the simulation-versus-measurement discrepancies are described. This Section also presents in some detail the models developed for the main functional blocks within the SCDC, including an analysis of simulation time required by these models in comparison with the transistor level representations of the corresponding blocks.

A. Top level description of the switched capacitor DC-DC converter

Figure 2 presents the simplified schematic of the switched capacitor DC-DC converter analyzed here. It consists of five main functional blocks, indicated by different colors in Figure 2.

The key element of the SCDC is the flying capacitor, C_{FLY}, which transfers charge between the supply voltage source, V_{BAT}, and the load capacitor, C_L. The charging and discharging of the C_{FLY} is enabled by the switch matrix, controlled by two non-overlapping phases, $\Phi1$ and $\Phi2$, of a fixed-frequency clock generated by an internal oscillator:

- during the $\Phi1$ phase switches S2 and S4 are ON and C_{FLY} gets charged by the Power Mirror formed by transistors M1 and M2.

- during the $\Phi2$ phase switches S1 and S3 are ON, connecting C_{FLY} in parallel with the load capacitor, C_L. The switch S5 is also ON, disabling the Power Mirror.

The output voltage is kept at a constant level, $V_{OUT} = V_{REF}(1 + R1/R2)$, by the control loop formed by the resistive divider R1-R2 and the *operational transconductor* (OTA), which supplies the input current to the Power Mirror. The reference voltage and bias currents are derived from a bandgap reference [6],[7].

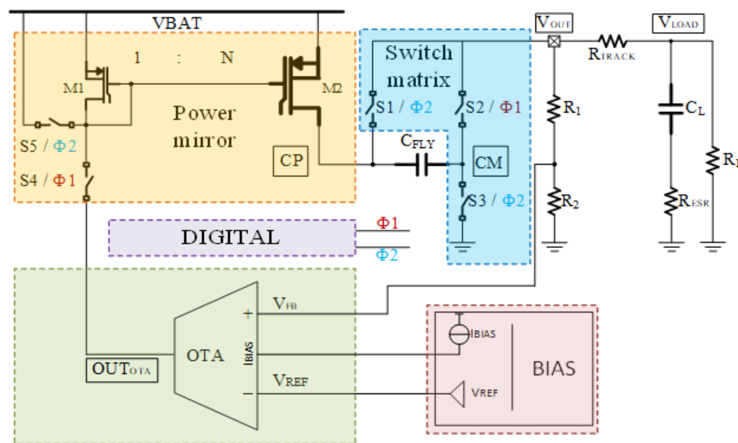

Fig. 2. SC DC-DC converter block diagram.

B. Problem description

Figure 3 shows the SCDC output voltage waveforms yielded by pre-silicon PEX simulations (top) and by post-integration measurements (bottom). There are obvious differences between the simulation and measurement results:

- during the Φ1 phase the simulation predicts a very small variation of the output voltage - about 6 mV, while measurements show a variation larger than 150 mV.

- during the Φ2 phase the simulation predicts a variation of the output voltage only slightly larger than for the Φ1 phase, of about 12 mV, while measurements show a variation of around 30 mV.

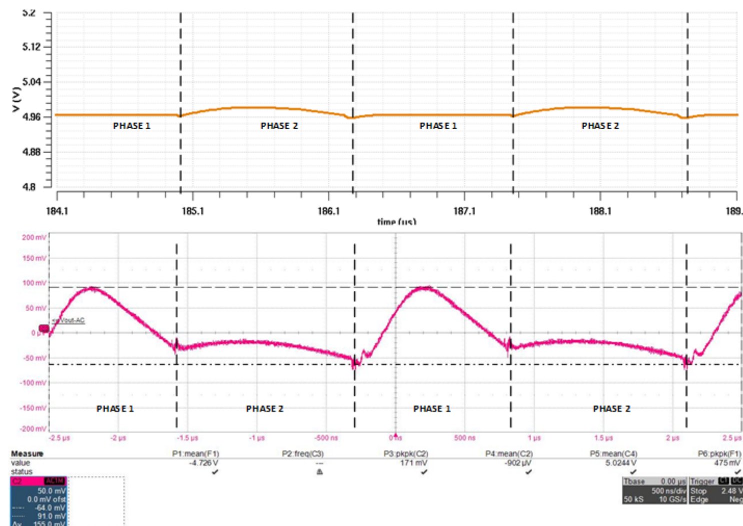

Fig. 3. Simulated (top) and measured (bottom) output voltage of the SC DC-DC converter shown in Figure 2. The measured waveform focuses on the output voltage ripple.

C. Development of behavioral models for the main functional blocks

Following the methodology described in Section II, we started the quest for finding the root-cause of the simulation-versus-measurement discrepancies shown in Figure 3 by developing Verilog- A models for the main functional blocks within the SCDC [8]. Of course, if the design flow had followed from the beginning the "top-down" methodology [9],[10], such models would have been already developed, and only minor adjustments might have been required.

The general design recommendation made in [11], [12] and [13] were followed to ensure convergence. Also, the models were tailored for simulations that mix schematic and/or model views of various parts of a system. Figure 4 illustrates the features/parameters modeled for each of the SCDC functional blocks by using standard SPICE primitives and components.

The development of behavioral models starts with simulation-based characterization of the corresponding blocks, focusing on the features and parameters of interest shown in Figure 4:

- "OTA": the input – output transfer function, $I_{OTA} = f(V_{DIFF}, OUT_{OTA})$, was derived by using DC sweep and the corresponding frequency characteristics were obtained by running AC simulations.
- "Power Mirror": only AC simulations were required to extract the frequency characteristics of the current mirror gain.
- "Switch Matrix": the ON resistances and the timing constants of the switches were obtained by running TR simulations.
- "Reference voltage and current sources": OP simulations were sufficient to derive the nominal values of the voltages and currents provided by this block, as well as the impedances corresponding to its outputs.

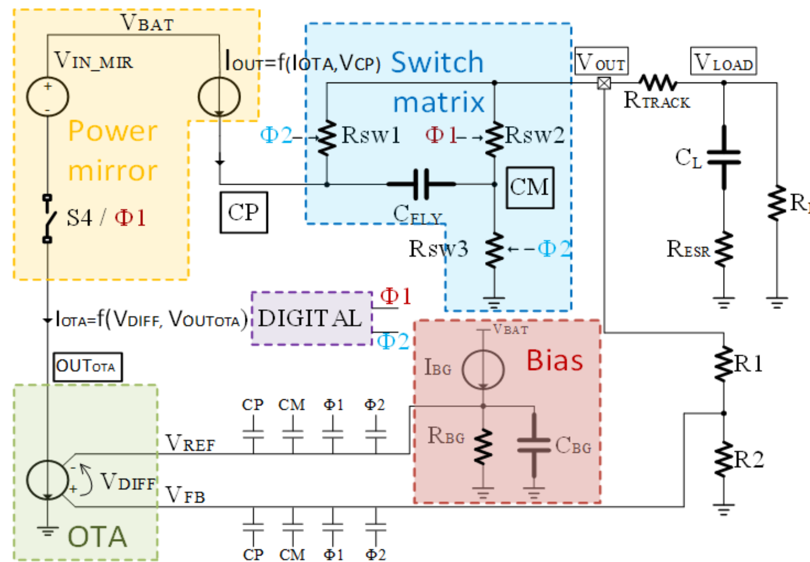

Fig. 4. The "tb_measurement" and the "schematic_top_parasitics" built for the SC DC-DC converter. It comprises: simplified representations of the behavioral models developed for the main functional blocks shown in Figure 2, capacitances for coupling the noise-sensitive lines V_{REF} and V_{FB} with the noisy nodes CP, CM, Φ1 and Φ2, the parasitic resistance of the OUT-LOAD track, Rtrack, and the R_{ESR} of the load capacitor.

1) Transconductance amplifier

The OTA, in normal operation mode, can be simply represented by a voltage controlled current source, as shown in Figure 4. The output current of the OTA is generated by an NMOS transistor, therefore only positive current values can be obtained. Our model also emulates the operation of the OTA when its output stage is driven into saturation (for low values of $VOUT_{OTA}$) and when the current path is interrupted (switch S4 turned off). These features can be achieved by using a fairly simple expression, as follows:

$$I_{OUTOTA} = Vx(V_{DIFF}) \cdot gm \cdot (1 - e^{-VOUT_{OTA}/Vz}) \quad (1)$$

where gm is the OTA transconductance, $VOUT_{OTA}$ is the OTA output voltage, Vz (equal to 6.3V) controls the knee of the I_{OUTOTA} curve which is limited due to output saturation. $Vx(V_{DIFF})$ is a function used to implement the nonlinear OTA characteristic, $I_{OTA} = f(V_{DIFF})$, shown in Figure 5, including its extreme regions (saturation and near zero output current). It can be expressed as follows [14]:

$$Vx = -ln(1+e^{-(V_{max}+V_{DIFF})/Vk1}) \cdot Vk1 - V_{DIFF} + ln(1+e^{(V_{min}+V_{DIFF})/Vk2}) + \cdot Vk2 \quad (2)$$

where $V_{DIFF} = V_{FB} - V_{REF}, V_{max} = I_{OUTOTA}_max/gm, V_{min} = I_{OUTOTA}_min/gm$. The limit of the upper and lower saturation regions can be set through factors $Vk1$ and $Vk2$. The characteristic shown in Figure 5 was obtained for $Vk1 = 20mV$ and $Vk2 = 3.33mV$. The smooth transitions between the linear and saturation regions is worth noting, as sharp transitions are often result in convergence problems.

The model frequency characteristic was obtained using the "laplace_nd" Verilog-A function [15], which takes as arguments the nominator and the denominator of an S-domain transfer function. Here, the transfer function comprised two poles and one zero.

The main features of this model are the DC transfer characteristic shown in Figure 5 and the AC transfer characteristics shown in Figure 6.

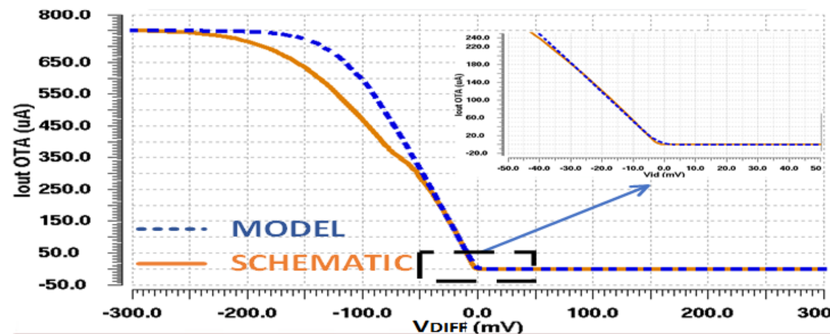

Fig. 5. OTA DC transfer function, $I_ota = f(Vdiff)$, obtained by running simulations on the actual schematic (continuous line) and the OTA model (dashed line) [8].

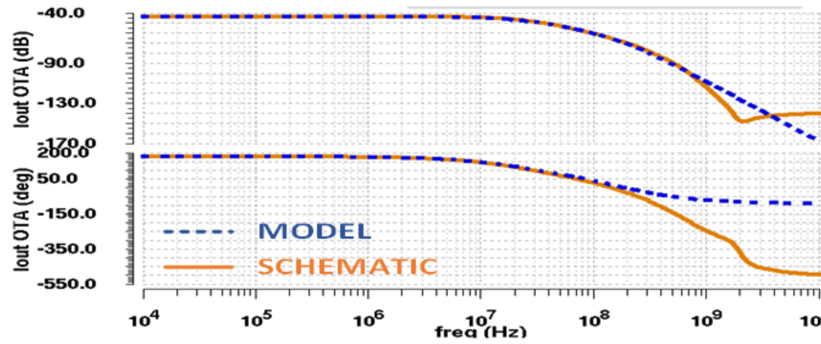

Fig. 6. Frequency characteristics of the OTA transconductance, obtained by simulations run on the "Schematic" (continuous line) and "Model" (dashed line) views of the OTA [8].

2) Power mirror

The simplest version of the power mirror model will only have to generate a scaled output current based on the input current value. For this, a simple current multiplication was enough. To get closer to the real behavior of the block, the scenario when the power mirror output is driven into saturation was modeled based on the following equation:

$$I_{OUTPM} = I_{IN} \cdot N \cdot (1 - e^{-(VOUT_{PM}/Vz)}) \tag{3}$$

where I_{IN} and I_{OUTPM} are the currents at, respectively, the input and the output of the power current mirror, N is the power mirror current gain. Vz controls the transition between the linear operation and saturation of the power mirror. By setting Vz to an appropriate value one ensures that the current mirror gain get smoothly compressed as the mirror enters saturation. $VOUT_{PM}$ represents the voltage drop across the power mirror output.

To mimic the frequency behavior of the schematic implementation a transfer function with a single pole was implemented by using the "laplace_nd" Verilog-A function. Figure 7 shows that the frequency characteristic of the model follows closely the frequency characteristic obtained by running PEX simulations up to 100MHz.

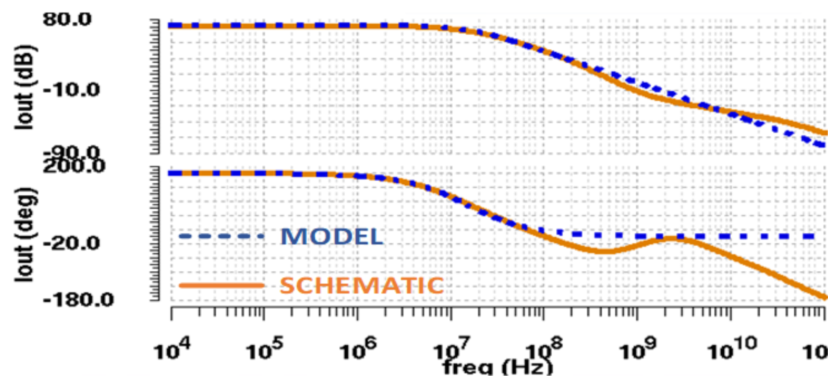

Fig. 7. Current Gain of the Power Mirror: frequency characteristics yielded by simulations run on the "Schematic" (continuous line) and "Model" (dashed line) views [8].

3) The switch matrix

The switch matrix consists of three switches, modelled by their equivalent ON/OFF resistance values, as shown in Figure 4. In order to improve convergence, the transition between ON and OFF values is made in a continuous manner using the following function [14]:

$$R_{sw} = R_{on} + R_{off}/(1 + e^{(Th-Vc)/Vk}) \tag{4}$$

where Rsw is the equivalent switch resistance, $Ron/Roff$ are the extreme ON/OFF resistance values (with Ron<<Roff), Th is the threshold of the control voltage, Vc, and Vk controls the transition between Ron and Roff values.

The appropriate values for the Vk and Th parameters were obtained experimentally, by comparing results obtained for transistor level representation of the entire SC DC-DC converter with results obtained by using the switch matrix model, as shown in Figure 5. The model includes the ON resistance of the switches and the dead-time (the period of time during which neither $\Phi1$ nor $\Phi2$ signal is active).

The turn ON/turn OFF time and ON/OFF resistance for the switches contained in the switch matrix block were obtained after several increments to an initial estimated value, aiming at matching model results to schematic ones. Figure 8 illustrates the results for the last step of this iterative process.

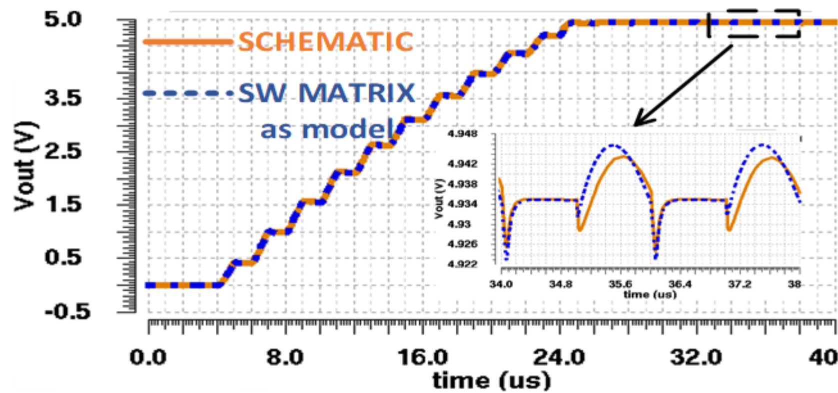

Fig. 8. Simulated output voltage of the SC DC-DC starting from power-up (t=0). Continuous line: simulations run on the actual schematic; dashed-line: simulations run with all blocks in schematic view except for the Switch Matrix which was represented by the model developed for it [8].

4) Simulation time

Simulations for the start-up test presented in Fig. 8 were run for three views of the SCDC top-level schematic, as follows:

- **Behavioral model** - the five sections indicated in Figure 4 represented by their models, previously described in this Section.
- **Schematic-only** - all blocks represented by their transistor-level schematics.
- **Schematic+PEX** – OTA and Power Mirror represented by their parasitic extracted views, with all other blocks represented by their transistor-level schematics.

Simulations using parasitic extracted views for more of the main blocks was not possible due to long simulation times or convergence issues.

Simulations were run on an average-level server, on which the standard Cadence-Virtuso software was installed. The Spectre simulator was used, with the standard accuracy settings: liberal, moderate and conservative.

First row of Table 1 presents the simulation times required when the "Behavioral model" was used. The simulation time for transient simulations run up to 200μs was 5 minutes for liberal accuracy, 11 minutes for moderate accuracy and 16 minutes for conservative accuracy.

The absolute values may not be relevant to the reader, as they depend on the simulation server performance, but they are useful as references. Thus, the next rows of Table 1 list the factors by which the simulation times of the "Behavioral model" need be multiplied by to get the corresponding simulation times for the Schematic-only and the "Schematic+PEX" representations of the SCDC. These multiplication factors range from 5 to 58. Note that simulation for the "Schematic+PEX" view run by using the conservative accuracy setting required a couple of days to complete; thus, this case was considered impractical and was excluded from this comparative analysis.

Table 1. First row: Time required to run the start-up transient simulation shown in Figure 8 up to 200μs for the "Behavioral model" representation of the SCDC, when three accuracy setting are used. Rows two and three: factors by which the simulation times of the "Behavioral model" need be multiplied by to get the corresponding simulation times for the "Schematic-only" and the "Schematic+PEX OTA and Power Mirror" representations of the SCDC

View used for simulation	Simulation Accuracy (Spectre Simulator)		
	Liberal	Moderate	Conservative
Behavioral model	Simulation time		
	5 minutes	11 minutes	16 minutes
	Time Multiplier wrt. Behavioral model, for same accuracy setting		
Schematic-only	x16	x5	x8
Schematic + PEX views for OTA and Power Mirror	x58	x12	-

4. Analysis of possible root-causes for discrepancies between simulation and measurement results

Parametric simulations were run on the "tb_measurements" testbench that included the "schematic_top_parasitics" view, as shown in Figure 4, in order to assess the sensitivity of the SCDC output voltage ripple. Following the strategy described in Section 2.C, block-level non-idealities were considered first, followed by non-idealities related to package and external components and, finally, internal parasitics such as capacitors coupled between key internal nodes. Representative examples of these simulations are presented in the followings. For readers convenience, all the simulation results presented here were obtained for the same use-case: V_{BAT} set to the typical value, 13V, the maximum load current, $ILmax = 200mA$. The switching frequency was set to 500kHz and $C_{FLY} = C_L = 1\mu F$.

A. Potential impact of non-idealities related to the main functional blocks

1) Effect of the ON resistances of the power switches

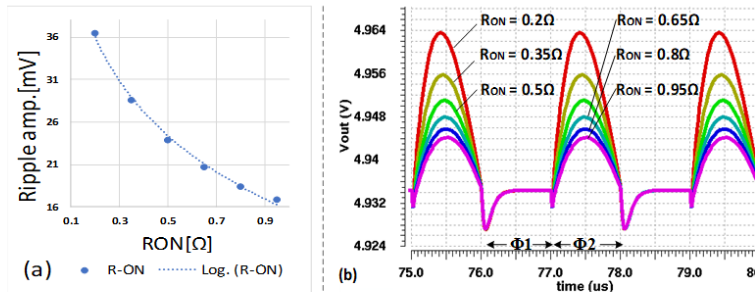

Fig. 9. Variation of the SCDC output voltage when the ON resistance of switches SW1-3 (RON) takes values between 0.2Ω and 0.95Ω: a). Ripple amplitude versus RON value and b). Output voltage waveforms. V_{OUT} ripple decreases from 36.5mVpkpk (RON=0.2Ω) to 16.9mVpkpk (RON= 0.95Ω).

Figure 9.b). presents the SCDC output voltage when the ON resistance of power switches was swept between 0.2 Ω and 0.95 Ω. They indicate that the ripple amplitude during phase Φ2 decreases logarithmically with the ON resistance, as shown in Figure 9.a), while the ripple corresponding to phase Φ1 is effectively insensitive to it. This result is in line with our expectations and indicates that this parameter is not the cause of the simulation-measurement discrepancies shown in Figure 3, wherein the measured ripple amplitude went up to 150mV during phase Φ1.

2) Non-overlap time between phase 1 and 2 (dead time)

Figure 10.b). presents the SCDC output voltage when the duration of the non-overlap period between phase 2 and phase 1 was swept between 20ns (the value indicated by PEX simulations performed at block-level) and 120ns. Figure 10.a). shows that the amplitude of the output voltage ripple during phase Φ1 increases linearly with the dead time value, reaching a maximum value of 36mV for 120ns dead time. However, this means that the dead-time value must be increased to an un-plausibly large value of 360ns in order to obtain the 150mV ripple amplitude seen in Figure 3. Moreover, Figure 10.b). shows that in this case the output voltage ripple is caused by a voltage undershoot during the non-overlap period, which again, is not similar to the measured waveform.

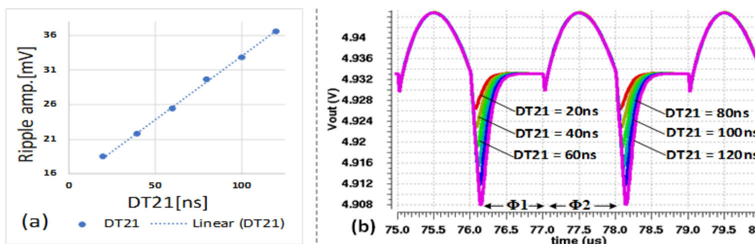

Fig. 10. Variation of the SCDC output voltage when the dead-time between Phases 2 and 1 (DT21) takes values between 20ns and 120ns: a). Ripple amplitude versus DT21 value and b). Output voltage waveforms. V_{OUT} ripple almost doubles, from 18.5mVpkpk (DT21=20ns) to 36.6mVpkpk (DT21=120ns).

B. Potential impact of non-idealities related to the external components

1) ESR of the load capacitor

Parametric simulations shown that the ESR of the load capacitor, CL, has an impact on the output voltage ripple. Figure 11.b). presents the SCDC output voltage when the ESR value was varied between 3mΩ and 125mΩ; Figure 11.a). shows that the amplitude of the output voltage ripple during phase Φ1 increases linearly with the ESR value, between $18.5mV_{pkpk}$ and $40.2mV_{pkpk}$. Again, these values are far lower than the measured ripple and the waveforms seen in Figure 11.b) have different shape compared to the measured output voltage shown in Figure 3. In fact, the ESR effect is related to the voltage undershoots that appear during dead-time.

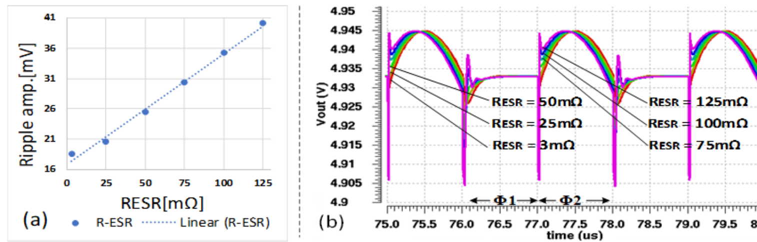

Fig. 11. Variation of the SCDC output voltage when the R_{ESR} of the load capacitor takes values between 3mΩ (Vout ripple $18.5mV_{pkpk}$) and 125mΩ (Vout ripple $40.2mV_{pkpk}$): a). Ripple amplitude versus R_{ESR} and b). Output voltage waveforms.

2) Output track resistance

The output track resistance was considered in this analysis because the feedback loop, controlling the output voltage level, had to be close inside the chip due to limited number of pins available. Therefore, the resistance of the track between the output pad and the external load – including the bondwire and PCB track – was expected to cause a DC shift of the output voltage, measured directly on the load, $C_L||R_L$. This is confirmed by parametric simulations shown in Figure 12. b), where parameter R_{TRACK} was swept between 1mΩ and 125mΩ.

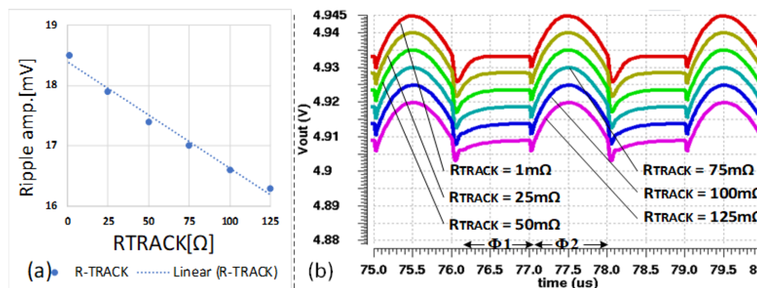

Fig. 12. Variation of the SCDC output voltage when the parasitic track resistance, R_{TRACK}, takes values between 1mΩ (VOUT ripple = 18.5mVpkpk) and 125mΩ (VOUT ripple = 16.3mVpkpk): (a) Ripple versus R_{TRACK}; (b) Output voltage waveforms.

Note that a value of 10mΩ was estimated based on PEX simulations and PCB calculations. Figure 12. a). shows that the amplitude of the output voltage ripple in phase $\Phi1$ decreases only slightly as the R_{TRACK} value increases, from 18.5mVpkpk to 16.3mVpkpk.

C. Potential impact of internal parasitic capacitances – coupling between noisy and sensitive lines

The effect of noise coupling was analyzed by sweeping the value of coupling capacitances connected between the noise-sensitive OTA inputs - lines V_{REF} and V_{FB} - and the noisy nodes CP, CM, $\Phi1$ and $\Phi2$ that exhibit large voltage swings, as shown in Figure 4.

Figure 13 presents the SCDC output voltage when the capacitance placed between node CP and the reference voltage, V_{REF}, was swept between 1fF and 15fF. The voltage during phase $\Phi1$ increases significantly with the value of this capacitor, so one can obtain the 150mV ripple amplitude seen in measurements for relatively small – thus plausible – values of the coupling capacitor.

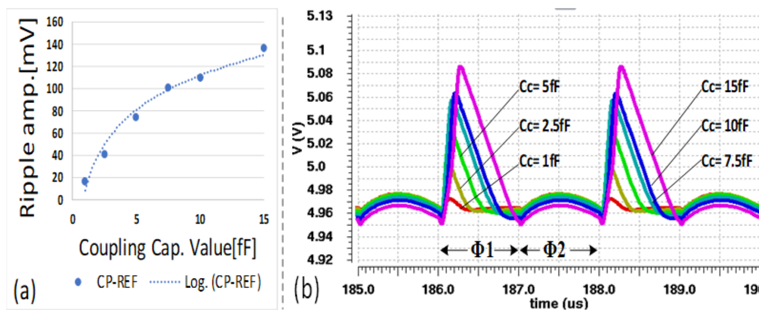

Fig. 13. Variation of the SCDC output voltage when the coupling capacitance between nodes CP and V_{REF}, C_{CP-REF}, takes values between 1fF (VOUT ripple = 16.8mVpkpk) and 15fF (VOUT ripple = 137mVpkpk): (a) Ripple amplitude versus coupling capacitance C_{CP-REF} and (b) Output voltage waveforms.

Figure 14 presents the SCDC output voltage when the value of capacitance placed between node CP and the other OTA input, V_{FB}, was swept between 1fF and 15fF. This time, the output voltage drops during phase $\Phi1$, in opposite behavior to the one observed in measurements.

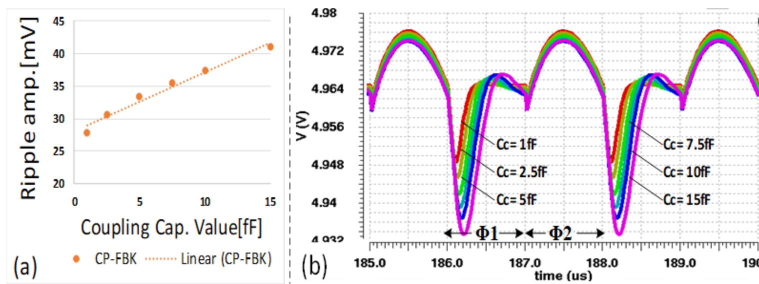

Fig. 14. Variation of the SCDC output voltage when the coupling capacitance between nodes CP and V_{FB}, C_{CP-FBK}, takes values between 1fF (VOUT ripple = 27.8mVpkpk) and 15fF (VOUT ripple = 41mVpkpk). (a) - Ripple amplitude versus coupling capacitance C_{CP-FBK} and (b) – Output voltage waveforms.

Figures 15 and 16 show simulation results similar to the ones presented in Figures 13 and 14. These were obtained by sweeping the values of coupling capacitors placed between the node CM and the OTA inputs, nodes V_{REF} and V_{FB}, respectively, between 1fF and 15fF. It can be noticed the impact these capacitors have on the output voltage ripple, even if their values are assumed to be relatively small.

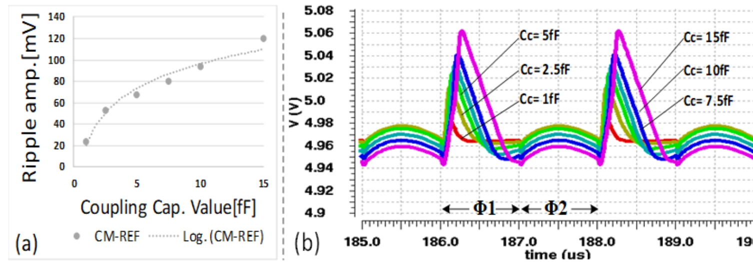

Fig. 15. Variation of the SCDC output voltage when the coupling capacitance between nodes CM and V_{REF}, C_{CM-REF}, takes values between 1fF (VOUT ripple = 23.5mVpkpk) and 15fF (VOUT ripple = 120mVpkpk). (a) - Ripple amplitude versus coupling capacitance C_{CM-REF} and (b) – Output voltage waveforms.

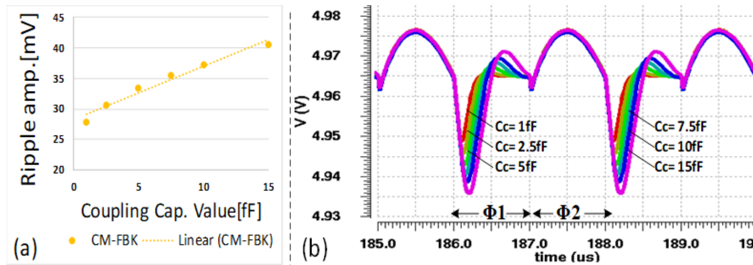

Fig. 16. Variation of the SCDC output voltage when the coupling capacitance between nodes CM and V_{FB}, C_{CM-FBK}, takes values between 1fF (VOUT ripple = 27.8mVpkpk) and 15fF (VOUT ripple = 40mVpkpk). (a) - Ripple amplitude versus coupling capacitance C_{CM-FBK} and (b) – Output voltage waveforms.

The simulation results shown in Figures 13-16 indicate that the reference voltage line V_{REF} is more sensitive to coupling with the noisy lines CP and CM than the feedback line, V_{FB}. This is also the case for coupling between the V_{REF} and V_{FB} lines and the clock phases, $\Phi 1$ and $\Phi 2$.

Figure 17 and Figure 18 present the output voltage ripple when the coupling capacitors placed between each of the clock phases, $\Phi 1$ and $\Phi 2$, and the reference line, V_{REF} are swept between 1fF and 15fF. One notices that the simulated output voltage waveforms shown in Figure 17.b) has a similar shape with the measured waveform shown in Figure 3. However, the simulated ripple amplitude is far smaller than the measured one. Therefore, this capacitive coupling is not the root-cause of the simulations-versus-measurements discrepancies we are looking for.

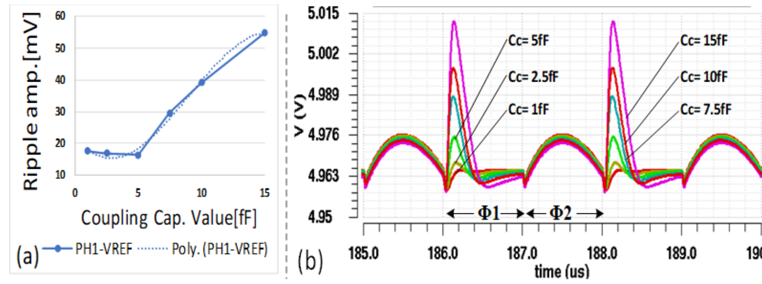

Fig. 17. Variation of the SCDC output voltage when the coupling capacitance between Φ1 and $V_{REF}, C_{PH1-REF}$, takes values between 1fF (VOUT ripple = 17.6mVpkpk) and 15fF (VOUT ripple = 54.8mVpkpk). (a) - Ripple amplitude versus coupling capacitance, $C_{PH1-REF}$ and (b) – Output voltage waveforms.

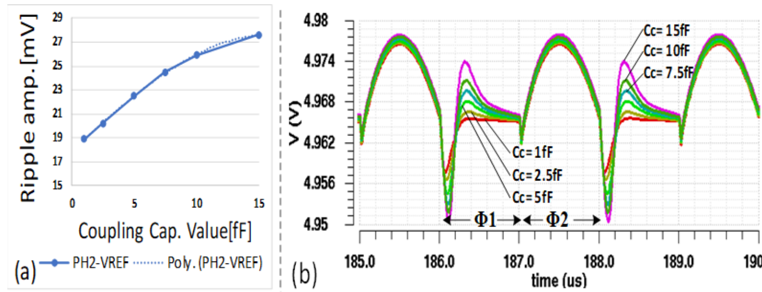

Fig. 18. Variation of the SCDC output voltage when the coupling capacitance between Φ2 and $V_{REF}, C_{PH2-REF}$, takes values between 1fF (VOUT ripple = 17.6mVpkpk) and 15fF (VOUT ripple = 54.8mVpkpk). (a) - Ripple amplitude versus coupling capacitance, $C_{PH2-REF}$ and (b) – Output voltage waveforms.

Table 2 presents a summary of the peak-to-peak voltage ripple at the SCDC output generated by the coupling capacitor connection place and value for the previous presented cases.

Table 2. Simulated amplitude of the output voltage ripple caused by capacitive coupling between various internal lines

Coupling scenario		Coupling capacitance value [fF]					
		1	2.5	5	7.5	10	15
Amplitude of output voltage ripple [mVpp]	CP-V_{REF}	16.8	41.2	74.6	101.7	110.7	137
	CP-V_{FBK}	27.8	30.6	33.5	35.6	37.5	41
	CM- V_{REF}	23.5	52.5	67.3	79.6	93.7	120
	CM-V_{FBK}	27.8	30.7	33.4	35.5	37.3	40.6
	Φ1-V_{REF}	17.6	17	16.4	29.6	39.2	54.8
	Φ2-V_{REF}	18.9	20.2	22.5	24.5	25.9	27.6

D. Identification of the root cause for simulations-measurements discrepancies

Simulations presented in the previous Section indicate that coupling between the CP and V_{REF} lines, and/or coupling between the CM and V_{REF} lines, are the most likely cause(s) of the simulation-versus-measurement discrepancies shown in Figure 3.

Next, the top-level layout of the SCDC was analyzed in detail, to ascertain whether the coupling between "suspected" lines mentioned above was indeed possible. Figure 19 presents a simplified representation of the SCDC, highlighting the "suspected" tracks. Note that the line which connects the reference voltage generated internally by the Bias block with the OTA input is also connected to the test pin V_{REF_EXT} via a T-pass-gate. This test pin was added in at the very last stage of the design as a fail-safe solution in case the internal bandgap failed. The track going to V_{REF_EXT} is narrow, but it crosses the wide track that connects the power mirror output with the CP pin – the wide horizontal track in the top-center of the IC. Moreover, the T pass-gate placed between it and the V_{REF} line was connected near the pin and was implemented with minimum-size transistors. Therefore, a large coupling capacitance appeared between lines CP and V_{REF}, whose value was eventually estimated to about 18.2fF. Similar analysis yielded a value of 0.5fF for the coupling capacitance that appeared between lines CM and V_{REF}, and values around 0.1fF and smaller for the other coupling capacitances.

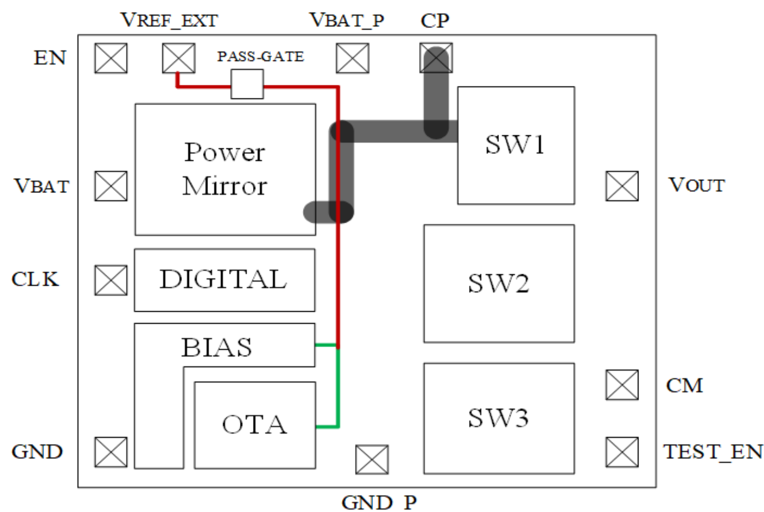

Fig. 19. The floorplan of the SCDC layout. The voltage V_{REF} generated by the BIAS block was routed to the OTA (green line) but the track was later extended to the pass-gate near the V_{REF_EXT} test pin (red line). The extended V_{REF} track passes over the wide CP track and an 18.2fF coupling capacitor appears between the two lines.

Figure 20 – top shows the SCDC output voltage obtained by running simulations on the "schematic_top_parasitics" view of the circuit with the coupling capacitances placed between V_{REF} and the lines CP and CM set to 18.2fF and 0.5fF, respectively, while the other coupling capacitors were set to 0.1fF. One notices that the resulting waveform is very similar, considering both the shape and actual voltage values, with the corresponding waveform obtained by measurements – shown at the bottom of Figure 20 for convenience.

Another test was performed to confirm this find: the V_{REF} line was driven by an external source connected to the test pin V_{REF_EXT} via a 100 Ω resistor while increasingly larger decoupling capacitors were connected between the V_{REF_EXT} pin and ground plane. This test confirmed the expectation that the amplitude of the output voltage ripple decreased when the spurs injected into the V_{REF} line by the CP and CM tracks were reduced through decoupling.

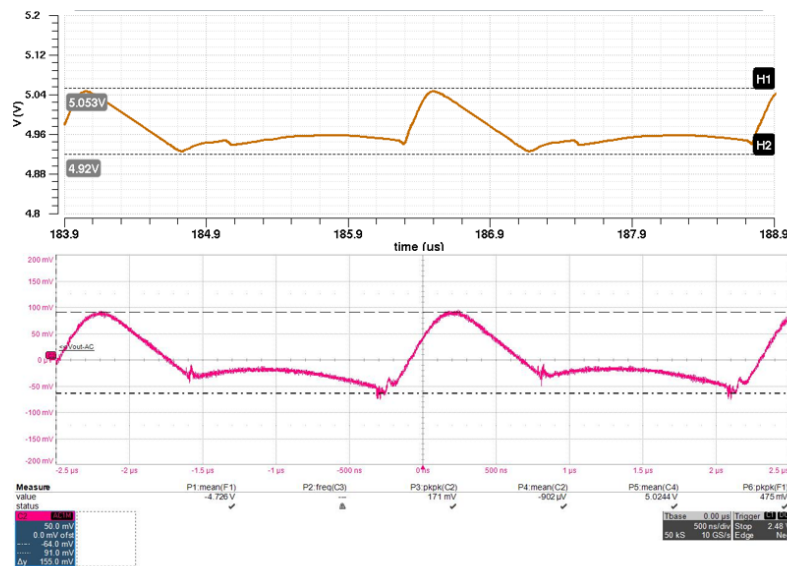

Fig. 20. SCDC output waveform: simulated with CCCP-to-V_{REF}=18.2fF included in the schematic (top) and measured (bottom).

5. Conclusions

This paper presents a methodology for ascertaining the root-cause of discrepancies between simulations and measurements related to a particular system parameter or feature. The main idea is to assess the sensitivity of that system parameter/feature to factors which may not have been accurately and comprehensively considered during pre-silicon verification, including block-level non-idealities, internal parasitic components and inaccuracies in modeling the package and/or the external components. As only a sensitivity estimate is necessary – as opposed to an accurate analysis - parametric simulations are sufficient: the value of each potential factor is swept within an appropriately wide range; the results indicate whether that factor has a strong enough impact on the IC performance to be considered among potential root causes or not.

After identifying the factors that impact the most the parameter/feature related to the simulation-versus-measurement discrepancy under analysis, the designer can find sets of values/combinations of some of those factors that yield simulation results most similar to the measurement results. Finally, the system layout, the simulation testbenches and the measurement setup are analyzed in detail, focusing on possible root cause(s) of the factors/combination of factors indicated by simulations.

This methodology relies on behavioral models for large functional blocks within the IC: the models not only reduce the netlist size – thus reducing the simulation time - but also allow the designer to analyze the effect some block-level non-idealities may have over the performance of the entire system. Other key factors are an amended version of the top-level schematic - that comprises the main parasitic components related to sensitive lines, such as voltage references, and noisy lines, such as those corresponding to nodes that swing fully between the supply rails – and amended testbench, that reflects as accurately as possible the measurement setup which includes parametric representations of package and external components non-idealities.

A real-life case of deploying the proposed methodology is presented in the paper: a switched-capacitor DC-DC converter, for which the measured output voltage ripple had a different shape and larger amplitude than those predicted by simulations. Parametric simulations indicated that the impact of external components and block-level non-idealities cannot reasonably explain the simulations-versus-measurements discrepancies; instead, they indicated the coupling between two noisy lines and a reference voltage line is the most likely explanation. Detailed analysis of the top-level layout confirmed that the parasitic capacitance between one of the "suspected" noisy line and the reference voltage line had a sufficient value to cause the output voltage ripple seen in measurements. This factor had not been detected in pre-silicon verification due to the relative small value of that parasitic capacitance – eventually estimated at 18.2fF – and because most of it appeared after the reference line was extended in order to implement a test mode added after the main design was completed.

The proposed methodology provides a systematic and effective approach to identifying possible causes of un-wanted behavior of large integrated circuits, for which it is not practical to run all simulations required by a comprehensive pre-silicon verification and/or for situations for which simulations are impacted significantly by inaccuracies in modelling integrated or external components.

In fact, sensitivity estimation based on behavioral models and parametric simulations should be included in the design flow of such ICs:

- parametrized behavioral models of key functional blocks are useful for deriving block-level parameters from general system requirements.

- the simple way of assessing potential impact of coupling between lines – by placing coupling capacitors between the lines and sweeping their values over reasonably wide ranges in parametric simulations – is very effective in setting clear requirements for layout routing of key tracks within the IC.

For this method to be efficient, the design team should be able to develop appropriate behavioral models. Simple functional models can be put together quickly, but it is important not to overlook second-order features that may prove important, such as non-linear transfer functions with saturation regions; also, continuous, smooth transition between operating regions is important, to avoid convergence problems. Detailed models require more time to develop, then to simulate. Finding the proper level of modelling detail for complex functional blocks is essential for the success of this method. It mostly relies on designers experience, but an iterative approach could yield good results for most cases: start with relatively simple – but not over-simplified to the point of uselessness – behavioral models, then expand them as the design progresses. Over time a design team can create its own library of generic models that can be used as starting points for future projects.

The main limitation of this method is that it does not guarantee the identification of root-cause of discrepancies between simulations and measurements in all cases. For example, let us consider the case whereby the root-cause is related to electro-thermal phenomena not considered by standard, electrical-only, simulators. Obviously, electro-thermal simulations are necessary, but it can be quite difficult to develop effective behavioral models for this case.

To conclude, we advocate for embedding the first steps of the proposed methodology into the design flow of mixed-mode integrated circuits, then using tailored behavioral models of functional blocks and simple representations of coupling between lines to speed-up top-level simulations for pre-silicon verification, and finally, to identify the root-cause of discrepancies between simulation measurement results.

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