

A Novel Full-Wave Current Sensor for Automotive Synchronous Buck Converters

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Abstract. This paper presents a novel full-wave current sensor based on the Vds-sense technique, suitable for fully integrated complementary switching power stages such as those used in synchronous buck DC-DC converters. It is designed to operate over a wide range of input voltages required by automotive applications. Provisions have been made for both current- and voltage-output, as well as for trimming. The novel sensor was derived by addressing the main limitations of a solution published previously by the authors. Both the circuit topology and circuit implementation were improved in order to increase the sensor accuracy. The new topology is simpler and allows for the signal paths to be implemented by using low-voltage transistors; the main transconductors were implemented by using the common-gate topology, which provides large bandwidth for a relatively low power consumption.

A design example is presented in some detail: a full-wave current sensor for synchronous buck DC-DC converter designed in a High-Voltage 180nm CMOS process. The converter provides a nominal 5V output and up to 500mA, while the input voltage varies between 6V and 45V. Simulation results shown that the current sensor presented here operates over the entire range of input voltages and resulting duty-cycle, between 10% and 80%. The relative error when the signals driving the power switches have a 50% duty-cycle is under 1.2%pkpk for inductor currents larger than 200mA and remains below 7.2%pkpk down to 50mA.

Key-words: Full-wave current sensor, Vds-sense, sense-FET, synchronous buck converter, Sample&Hold, common-gate amplifier.

1. Introduction

Accurate sensing of the current flowing through an inductor is required by many power management and control applications, ranging from DC-DC converters to adjustable speed motors drivers. Of the many techniques proposed so far, the sense-FET or Vds-sense is the most popular

choice for fully integrated sensors [1–5]. It relies on sensing the voltage drop across MOS power switches turned ON. For this, the same voltage is forced to appear between the drain and source of a sense transistor - that is, a scaled-down replica of the power switch - whose gate is held at the same potential as the switch gate. The current sensing accuracy depends on ensuring that the drain-source and the gate-source voltage of the power switch and the sense transistor are equal.

Fig. 1 presents the block diagram of a synchronous buck DC-DC converter with average current mode control [6]. A full-wave current sensor is required to monitor the current flowing through the inductor, that also flows alternatively through the power switches: the PMOS transistor M_P in the High-Side conduction mode and the NMOS transistor M_N in the “Low-Side” conduction mode. The Vds-sense technique, depicted in Fig. 1 within the shadowed rectangle, is based on the “sense” transistors, M_{PS} and M_{NS} , that are K-times smaller replicas of the power switches, M_P and M_N . The active elements within the block denoted CSE ensure that the drain-source voltage, Vds, of each sense transistor follows closely the Vds of its corresponding power switch. Thus, K-times smaller replicas of the currents flowing through M_P and M_N appear at the drains of transistors M_{PS} and M_{NS} , which are further processed by the CSE block to produce the output current $I_{OUT} = I_L/K$.

Recently, a novel topology for implementing full-wave current sensors have been reported [1]; it was derived from the topology proposed in [2] by addressing the main shortcomings of the later, that hindered its accuracy. This paper presents a full-wave current sensor similar to, but significantly improved compared to, the sensor reported in [1]. The improvements described here refer to both sensor topology and its circuit implementation. The goal is to ensure a better accuracy over a wider range of load currents, but also to implement additional features, such as trimmable output current or output voltage.

Section II describes briefly the topology and circuit implementation of the current sensor reported in [1] and analyses the main factors that limit its accuracy. Section III presents the improved current sensor proposed here, focusing on the topology improvements that address some of the limitations identified for the sensor topology used in [1] and allow for a simpler, more effective, circuit implementation. New transistor-level schematics of key circuits are also presented. A design example is presented in Section IV that demonstrate the effectiveness of the new solution: the current sensor described in Section III was designed in the same 180nm High-Voltage CMOS process and to the same requirements as the one in [1], as part of a buck converter with input voltage ranging from 6V to 45V. The performance of the resulting circuit is compared against the performance of solutions reported in [1], [2] and [3]. Conclusions and drawn in the final Section.

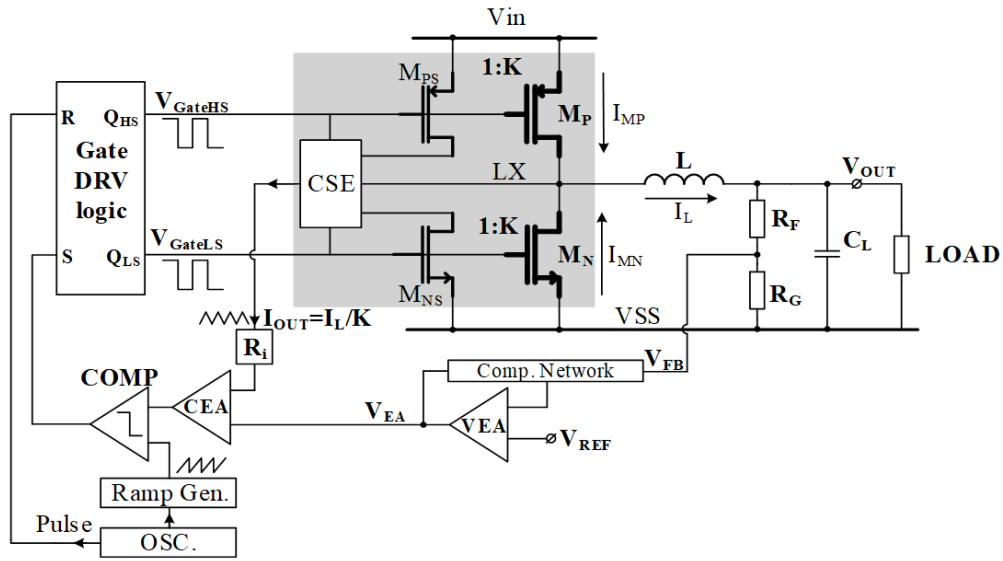


Fig. 1. Block diagram of a Synchronous Buck with average-current mode control, with key elements of the full-wave current sensor based on the V_{ds} -sense technique: the “sense” transistors, M_{PS} and M_{NS} , that are K -times smaller replicas of the power switches, M_P and M_N . The active elements within the block denoted CSE ensure that the drain-source voltage, V_{ds} , of each sense transistors should follow closely the V_{ds} of its corresponding power transistor.

2. Brief analysis of the full-wave current sensor reported in [1]

a. Topology and main functional equations

Fig. 2.b presents the block diagram of the full-wave current sensor reported in [1], side by side with the one introduced in [2], which is shown in Fig. 2.a. The topology reported in [1] brought in four important improvements compared to the structure described in [2]:

- high-input impedance Gm cells were used, which allowed the number of configuration switches to be reduced, from seven to four;
- the outputs of the Low- and High-Side parts of the sensor were combined by using the PMOS current mirror M1-M2, with no systematic mismatch;
- the Sample&Hold circuit formed by MS5, MS6 and Cs did not break the feedback loop formed by M2. It simply allowed the current mirrored by M1 to be updated only after the current through M2 had settled;
- the two bias current sources i_b ensured that transistor M2 was always ON, even if the inductor current went negative.

Fig. 3.a presents the section of the circuit shown in Fig. 2.b which is active when the sensor operates in the High-Side mode. One notices that the current provided by the sense transistor M_{PS} is split evenly between M1 and M2. Assuming that transconductors Gm1 and Gm2 have large input impedances, the current outputted by the current sensor when operating in this mode has the following expression:

$$I_{CORE_HighSide} = I_{dMP} \frac{R_{dsMP}}{2R_{dsMPS}} + i_B \frac{R_{dsMS2}}{2R_{dsMPS}} \quad (1)$$

where I_{dMx} and R_{dsMx} are the drain current and drain-source resistance of transistor Mx. Fig. 3.b presents the circuitry active when the sensor operates in the Low-Side mode. This time, the entire current provided by the Low-Side sense transistor M_{NS} flows through transistor M2. Thus, the current outputted by the sensor when operating in this mode is equal to the drain current of M2, mirrored by M1 without scaling. Under the same conditions considered for the High-Side case – transconductor Gm2 having large input impedances – the Low-Side core current has the following expression:

$$I_{CORE_LowSide} = I_{dM2} = I_{dM1} = I_{dMN} \frac{R_{dsMN}}{R_{dsMNS}} + i_B \frac{R_{dsMS3}}{R_{dsMNS}} \quad (2)$$

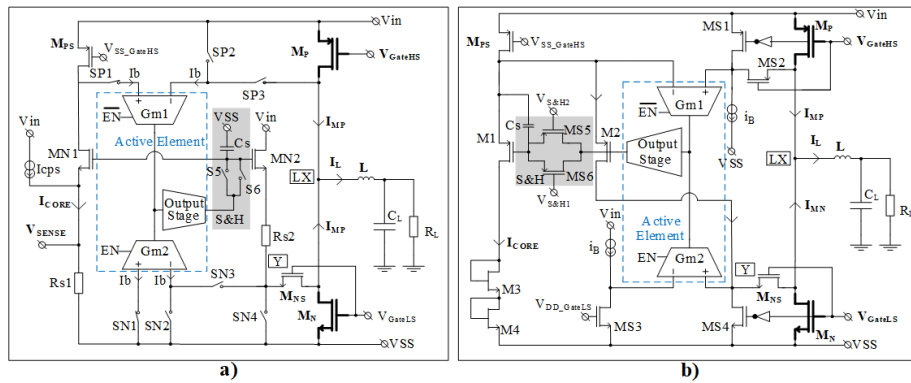


Fig. 2. Block diagram of the full-wave current sensor for synchronous buck converter reported in [2] – figure a)- and in [1] – figure b). The Active Element (AE) – that comprises transconductors Gm1 and Gm2 and their common output stage – is included in a dotted rectangle while the Sample&Hold circuit is placed in a shadowed rectangle.

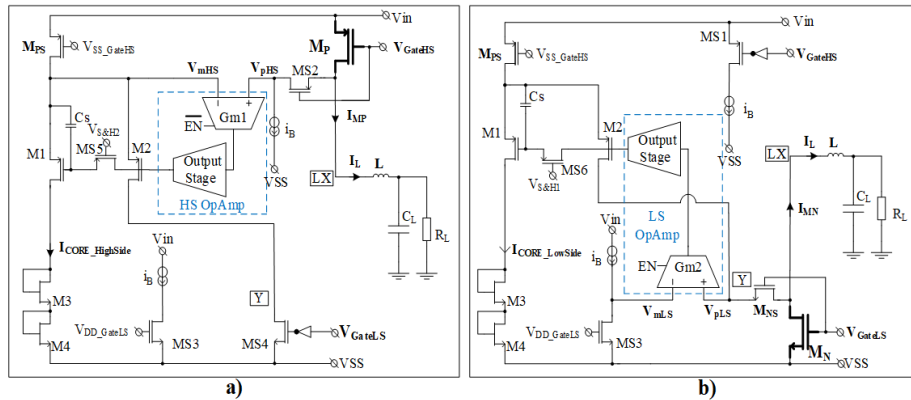


Fig. 3. The active part of the circuitry shown in Fig. 2.b when the proposed current sensor operates in the High-Side sampling mode (a) and in the Low-Side sampling mode (b) [1].

and dynamic non-idealities. The main factors that negatively impact the accuracy are:

- mismatches between the power switches and the sense transistors; - systematic and mismatch-related offsets within the main current mirror implemented by M1-M2. Note the large difference between the drain-source voltages of transistors M1 and M2;

- the offset voltages and bias currents of transconductors Gm1 and Gm2, as well as the finite gain value of the OpAmps formed by these transconductors, their common output stage and transistors M1 and M2, as shown in Fig. 3;

- the GBW of these OpAmps is relatively low, around 1MHz. Also, the settling time following their periodic enable/disable cycle, synchronized with the power switches control, is relatively long, well over 100ns. This is caused by the topology shortcomings described above and by the relative complex Active Element implementation shown in Fig. 4;

- high-voltage transistors driven by rail-to-rail control signals have to be used to implement the Sample&Hold circuit. The resulting clock feedthrough and channel charge injection, [8–9], impact significantly the sensor accuracy.

These shortcomings are addressed by the current sensor proposed in this work, described in the next Section.

3. Proposed full-wave current sensor: circuit implementation and main advantages

a. Circuit topology and compensation of static errors

Fig. 5 presents the block diagram of the full-wave sensor proposed in this paper. The circuit topology is similar to the one introduced in [1], shown in Fig. 2.b, but there are several key differences:

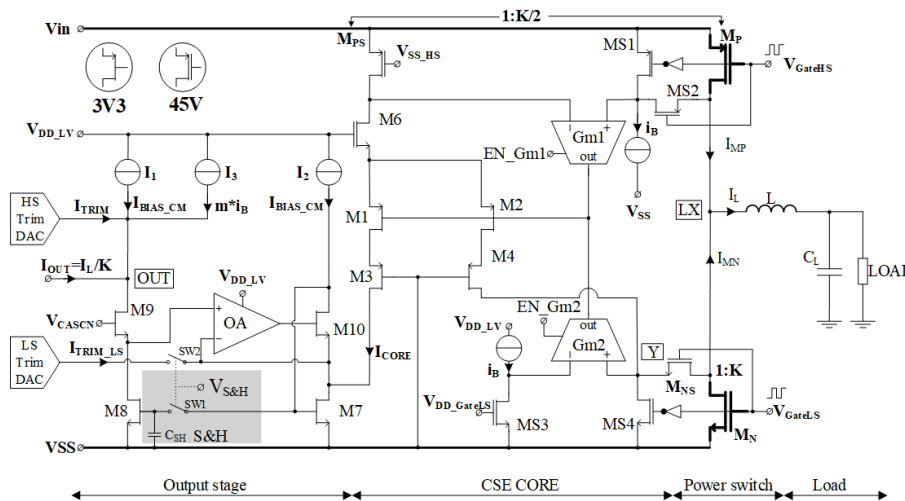


Fig. 5. Topology of the full-wave current sensor with current output proposed here. The thick-oxide, high-voltage transistors are highlighted. One notices that, with the sole exception of M6 and sense transistors, all signal paths within the sensor – including the two transconductors - can be implemented with thin-oxide transistors.

– the output stage is implemented by a current mirror with high output resistance and low input voltage. The later feature allows for the cascoding of the main current mirror M1-M2 – see transistors M3 and M4 in Fig. 5;

– the Sample&Hold circuit is embedded within the output current mirror, thus avoiding two shortcomings of the circuits reported in [1] and [2]: the Sample&Hold circuit in Fig. 5 is placed outside the feedback loops closed around transconductors Gm1 and Gm2, and it can be implemented with low-voltage transistors, driven by low-voltage logic supplied by the $V_{DD.LV}$ line, thus reducing clock feedthrough and channel charge injection;

– a high-voltage transistor, M6, was placed between the sense transistor M_{PS} and the current mirror transistor M1. This change has two major benefits: first, the main current mirror can be implemented with low-voltage transistors, as M1-M4 are insulated from the supply voltage, V_{in} , by the high-voltage cascode M6. The cascoded current mirror implemented with thin-oxide transistors presents a far smaller capacitive loading than its counterpart in Fig. 2. Second, transistor M6 implements a non-inverting gain stage in the feedback loop closed around Gm1;

– the common output stage shown in Fig. 2 is no longer necessary for the new topology presented in Fig. 5: in this case, transconductors Gm1 and Gm2 need to drive only a relatively small capacitive load and not the entire Sample&Hold circuit. Also, the M6 gain stage provides sufficient gain within the feedback loop closed around Gm1 in High-Side operation. Note that the feedback loop closed around Gm2 also comprises a gain stage, implemented by M2 in Low-Side operation.

The core of the circuit depicted in Fig. 5 operates similarly to the circuit reported in [1], described in Section 2. Thus, the core circuit sections active in High-Side and Low-Side modes correspond to those depicted by Fig. 3 and the core output current has expressions similar to the ones given by eq. (1) and (2), repeated here for convenience:

$$\begin{aligned}
I_{CORE_{HighSide}} &= I_{dMP} \frac{R_{dsMP}}{2R_{dsMPS}} + i_B \left(\frac{R_{dsMS2}}{2R_{dsMPS}} \right) \\
I_{CORE_{LowSide}} &= I_{dMN} \frac{R_{dsMN}}{R_{dsMNS}} + i_B \left(\frac{R_{dsMS3}}{R_{dsMNS}} \right)
\end{aligned} \tag{3}$$

where I_{dMx} and R_{dsMx} are the drain current and drain-source resistance of transistor Mx.

One can size the sense transistors so that the High- and Low-Side sections yield the same core current for a given value of the load current I_L :

$$\frac{R_{dsMP}}{2R_{dsMPS}} = \frac{R_{dsMN}}{R_{dsMNS}} = \frac{1}{K} \text{ and } \left(\frac{R_{dsMS2}}{2R_{dsMPS}} \right) = \left(\frac{R_{dsMS3}}{R_{dsMNS}} \right) = m \tag{4}$$

$$\Rightarrow I_{CORE_{HighSide}} = I_{CORE_{LowSide}} \approx I_L/K + m * i_B \tag{5}$$

The value of the bias current i_B is set considering the trade-off between maintaining a good accuracy even at low values of the inductor current and the total current consumption.

The output stage of the current sensor shown in Fig. 5 consists of the current mirror implemented by the transistors M7–M10 and the Operational Amplifier denoted OA, the DC current sources $I_1 - I_3$ that help remove the DC components of the mirrored current I_{CORE} , and two

current-output Digital-to-Analog Converters (DACs) used for trimming. Assuming a perfect current mirroring and the complete removal of the DC component, the current outputted by the sensor is proportional to the load current:

$$I_{OUT} = I_L/K \quad (6)$$

In principle, the accuracy of this sensor is limited by the same factors that negatively impact the sensor reported in [1], which were discussed in Section 2.b. However, several provisions have been made to diminish the impact these factors have and improve the accuracy of the sensor proposed here, such as:

- the systematic offset of the main current mirror was reduced by cascading transistors M1-M2 with M3-M4;
- the effect of static errors of the two OpAmps shown in Fig. 5 - formed by transconductors G_{m1} or G_{m2} , the main current mirror M1-M2 and the gain stages M6 and M2, respectively – can be reduced by trimming. This is implemented by the two current-output DACs placed at the very output of the Fig. 5 circuit; trimming will be detailed at the end of this sub-section;
- the dynamic performance of the main OpAmps mentioned above can be improved significantly compared to the corresponding OpAmps in Fig. 2.b, without increasing the power consumption. This is due to their simpler structure – no common output stage and no Sample & Hold circuit within the feedback loop – and their implementation with low-voltage transistors, with only one exception - transistor M6.

Fig. 6 presents a voltage-output version of the current sensor proposed in this work. The current yielded by the circuit shown in Fig. 5 is taken in by the current-to-voltage converter implemented by OA2 and R_{OUT} . Assuming a perfect current mirroring of I_{CORE} , perfect matching of current sources I_1 and I_2 , and perfect scaling of current i_B by the current source I_3 , the voltage outputted by this sensor is proportional to the load current:

$$V_{OUT} = R_{OUT} \frac{I_L}{K} + (V_A - R_{OUT} * I_{TRIM}) = \frac{I_L}{G_{m_Sensor}} + V_{REF} \quad (7)$$

where $G_{m_Sensor} = K/R_{OUT}$ is the overall current to voltage gain of the sensor and $V_{REF} = V_A - R_{OUT} * I_{TRIM}$ is the reference DC level set at the output for zero inductor current.

One can minimize the effect of mismatches inherent to an integrated implementation, as well as the static errors mentioned above, by adjusting the value and sense of I_{TRIM} . Trimming involves two steps, both performed with the load current set to zero: first, the sensor is forced to operate in the High-Side mode and the value of I_{TRIM_HS} provided by the High-Side DAC is adjusted until V_{OUT} is equal, or close to, the wanted V_{REF} value; second, the sensor is forced to operate in the Low-Side mode and the value of I_{TRIM_LS} provided by the Low-Side DAC is adjusted until V_{OUT} is equal, or close to, V_{REF} value. Note that the I_{TRIM_LS} current is added to I_{CORE} only when the sensor operates in Low-Side mode, correlated with the operation of the Sample&Hold circuit.

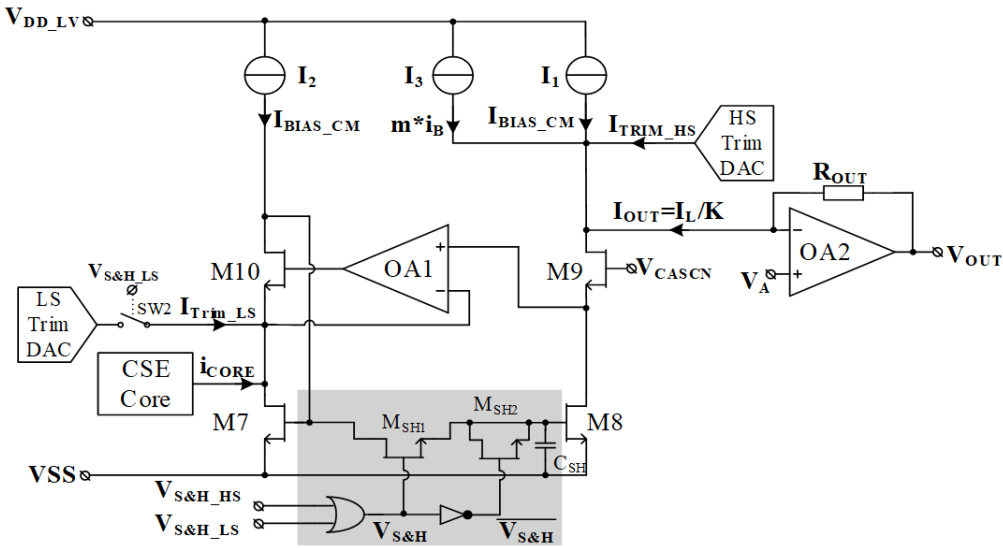


Fig. 6. A voltage-output version of the current sensor shown in Fig. 5. OA2 and R_{out} implement a current-to-voltage converter that provides an output voltage proportional to I_{OUT} , thus to the sensed load currents. An effective implementation of the Sample&Hold circuit is shown within the shadowed rectangle.

b. Improved implementation of the Sample & Hold circuit

In general, the power switches of a complementary power stage are driven by non-overlapping signals, to avoid simultaneous conduction of the switches. Large current spikes may appear during transitions between Low-Side and High-Side conduction, which can disrupt the control circuitry if reflected by the current sensor. This can be avoided by using Sample&Hold circuits, set to operate in the Hold mode during transitions [1–2].

An effective implementation of the Sample&Hold circuit used by the sensors proposed here is presented in Fig. 6, within the shadowed rectangle. It consists of a switch implemented by transistor M_{SH1} , and the dummy transistor M_{SH2} , the memory capacitor C_{SH} and the logic circuitry driven by the control signals $V_{S\&H_HS}$ and $V_{S\&H_LS}$. In order to help suppress clock feedthrough and minimize channel charge injection [8] the signal driving the dummy transistor M_{SH2} is complementary to the one that drives the M_{SH1} switch, and the size of the dummy is half the size of the switch.

When one of the control signals $V_{S\&H_HS}$ or $V_{S\&H_LS}$ are high, the circuit operates in the Sample mode: the M_{SH1} switch is turned ON and transistors M7-M8 implement a current mirror. When neither control is high, the switch M_{SH1} is turned OFF and the source current-mirror transistor, M8, is disconnected from the diode-connected M7. Thus, the output current is kept at a constant value by the voltage maintained by the memory capacitor C_{SH} at the gate of M8. The control signals $V_{S\&H_HS}$ and $V_{S\&H_LS}$ are pushed high only after the corresponding power switch – M_P and M_N – are fully turned ON and they are pulled down just before the turning OFF of the power switches starts. This avoids signal spikes at the sensor output caused by the transition between High- and Low-side modes of operation.

Figure 7 presents the chronograms of the main signals within the buck converter and the

current sensors presented here. The rise and fall times of the power stage gate signals from this figure are enlarged in order to highlight the transition points of the enable and Sample&Hold signals. For this reason, the Hold intervals appear wider than in real life, where they only account for around 10% of a $2\mu\text{s}$ period.

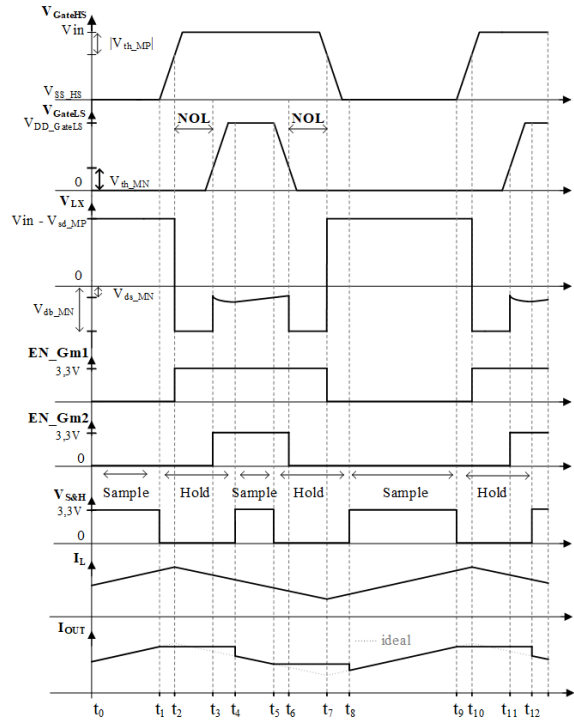


Fig. 7. Chronograms of main signals within the buck converter and the current sensor proposed here, shown in Fig. 5.

At the initial time - denoted t_0 in Fig. 7 - the Buck converter has reached a steady state, the power stage is set in High-Side conduction phase and the current sensor operates in High-Side Sample mode. During the $t_0 - t_1$ time interval the sensor monitors continuously the inductor current and outputs a current proportional to it, as predicted by eq.(6).

At the time marked t_1 , just before the High-Side power switch M_P is switched off, the control signal $V_{S\&H}$ is pulled down and the sensor enters the Hold operation mode. Such “early” signals are usually available at the input of the gate driver. As $V_{S\&H} = “0”$ during the Hold mode, the switch M_{SH1} is off and the source current-mirror transistor, M8, is disconnected from the diode-connected M7. Thus, the output current is kept at a constant value by the voltage maintained by the memory capacitor C_{SH} at the gate of M8. The size of the capacitor C_{SH} directly impacts the bandwidth of the sensor and the switching noise.

The time marked t_2 indicates the moment transconductor Gm1 is disabled pulling down the control signal EN_Gm1. At this moment the M_P is fully turned off, and the inductor current reaches the peak value. During the $t_2 - t_3$ time interval both power switches are OFF, and the switching node V_{LX} fall below 0V as the bulk-drain diode of M_N gets forward biased in order to ensure a current path for the inductor current. This time interval is known as non-overlap (NOL)

or dead time. The sensor is kept in the Hold operation mode, because the drain-source voltage of the Low-Side switch, M_N , is determined by the bulk-drain junction forward voltage and not by the $R_{dsMNS} * I_L$ product.

The time marked t_3 indicates the end of the NOL interval, when the gate-source voltage of the low-side switch, denoted V_{GateLS} in Fig. 7, reaches the threshold voltage of M_N , and the inductor current starts flowing through the drain-source channel of M_N . At this time, the control signal EN_Gm2 goes high, enabling transconductor Gm2. During the $t_3 - t_4$ time interval the gate voltage of V_{GateLS} continues to increase but the sensor is kept in the Hold operation mode because the gate charge migration can impact its accuracy. Moreover, both the transconductor Gm2 and the feedback loop closed around it needs some time to reach steady state.

At the time marked t_4 , when the V_{GateLS} reaches its steady state and M_N is fully ON, the Low-Side Sample operation mode is enabled by raising the $V_{S\&H}$ control signal. This signal is a delayed version of the actual signal that drives the gate of M_N . During the $t_4 - t_5$ time interval, the sensor monitors continuously the inductor current and outputs a current proportional to it, as predicted by eq.(6).

At the time marked t_5 , just before turning off the Low-Side power M_N , the signal $V_{S\&H}$ is brought down again, and the sensor returns to the Hold operation mode. The output current is kept at a constant value, set by the voltage maintained by the memory capacitor CSH at the gate of M8.

At the time marked t_6 , when the gate voltage V_{GateLS} drops below the threshold of M_N , transconductor Gm2 is disabled. This point marks the start of the second NOL interval where both power switches are turned OFF, which extends until the time marked t_7 . During the NOL period, the voltage at the switching node, V_{LX} , drops back to the voltage level determined by the forward voltage of the bulk diode. The sensor continues to operate in the Hold mode.

At the time marked t_7 , when the gate voltage V_{GateHS} is low enough to start turning ON the M_P power switch, the transconductor Gm1 is enabled by pushing high the EN_Gm1 control signal. This point marks the minimum inductor current and the end of the second NOL interval. The sensor is maintained in the Hold operation mode until both the V_{GateLS} and V_{LX} voltages reach their steady state. This also allows transconductor Gm2 and the feedback loop closed around it to reach steady state.

At the time marked t_8 the High-Side Sample operation mode is enabled by pushing high the $V_{S\&H}$ control signal and a new cycle starts.

c. Improved implementation of the active elements

As discussed in Section 2.c, the settling time of the OpAmps formed around transconductors Gm1 and Gm2, following their periodic enable/disable cycle, has a major impact on the dynamic errors of the current sensor. In principle, the settling time can be reduced by increasing the slew-rate (SR) and the gain-bandwidth (GBW) of these OpAmps. Analyses reported in [10] and [5] indicate that GBW values around 10MHz and settling times between 20ns and 90ns are necessary for buck converters with switching frequencies in the 500kHz – 2MHz range.

The circuit topology proposed in Fig. 5 makes it easier to obtain larger SR values than the one reported in [1], as here both transconductors Gm1 and Gm2 only drive relatively small capacitive loads. It is also better suited for large GBW values, as both transconductors and most of the signal paths can be implemented with thin-oxide transistors.

The common-gate topology is an increasingly popular option for implementing fast transconductors; it has been used in a wide range of power management applications, from error ampli-

fiers in LDOs with fast response to load and line transients [11] to current sensors [4] and [5].

Fig. 8 presents transistor level implementations of transconductors $Gm1$ and $Gm2$ shown in Fig. 5. For each of them, the inputs are connected to the sources of transistors $M1$ - $M2$, that operate in a straightforward common gate connection. Each input stage is cascoded by transistors $M3$ - $M4$ and is biased by cascoded current sources implemented by transistors $M7$ - $M8$. A second level of cascoding, implemented by transistors $M9$ - $M10$ is used to further increase the output impedances of these transconductors. In the case of transconductor $Gm1$, $M9$ - $M10$ are high-voltage transistors, able to withstand drain-source voltages of up to 45V. The disabling of these transconductors is achieved by switches $M11$ - $M12$.

One notices that both transconductors exhibit an unusually large input bias current – in fact, equal to the main biasing current, i_B . Usually a drawback, this actually suits the circuit topology proposed here: the bias current sunk by the positive input of $Gm1$ implements the current source i_B shown in Fig. 5 between that input and V_{SS_LS} , while the bias current sourced by the negative input of $Gm2$ implements the current source i_B shown in Fig. 5 between that input and V_{DD_LV} .

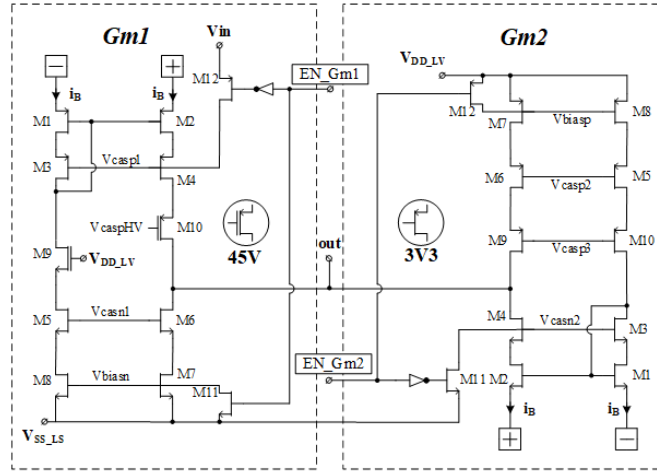


Fig. 8. Transistor level implementations of transconductors shown in Fig. 5, based on the common-gate topology. Left: $Gm1$, that is enabled in High-Side operation. Right: transconductor $Gm2$, which is enabled in Low-Side mode.

However, the bias currents present at the other inputs of transconductors $Gm1$ and $Gm2$ appear as additional currents flowing through the sense transistors M_{PS} and M_{NS} . Therefore, the currents yielded by the core of the current sensor have slightly different expressions that those given by eq.(3):

$$\begin{aligned} I_{CORE_{High-Side}} &= I_{dMP} \frac{R_{dsMP}}{2R_{dsMPS}} + i_B \left(\frac{R_{dsMS2}}{2R_{dsMPS}} - \frac{1}{2} \right) \\ I_{CORE_{Low-Side}} &= I_{dMN} \frac{R_{dsMN}}{R_{dsMNS}} + i_B \left(\frac{R_{dsMS3}}{R_{dsMNS}} - 1 \right) \end{aligned} \quad (8)$$

where I_{dMx} and R_{dsMx} are the drain current and drain-source resistance of transistor Mx .

The sense transistors can be sized so that the core output current yielded by the High-Side

section for the load current I_L matches the one yielded by the Low-Side section for the same load current, similarly to the case discussed in Section 3.a.

$$\text{If } \frac{R_{dsMP}}{2R_{dsMPS}} = \frac{R_{dsMN}}{R_{dsMNS}} = \frac{1}{K} \text{ and } \left(\frac{R_{dsMS2}}{2R_{dsMPS}} - \frac{1}{2} \right) = \left(\frac{R_{dsMS3}}{R_{dsMNS}} - 1 \right) = m \quad (9)$$

$$\Rightarrow I_{CORE_{HighSide}} = I_{CORE_{LowSide}} \approx I_L/K + m * i_B \quad (10)$$

As both the power switches, M_N and M_P , and their corresponding sense transistors, M_{NS} and M_{PS} , operate in the linear (triode) region, eq. (9) can be rewritten as follows:

$$K = \frac{\left(\frac{W}{L}\right)_{MP}}{2\left(\frac{W}{L}\right)_{MPS}} = \frac{\left(\frac{W}{L}\right)_{MN}}{\left(\frac{W}{L}\right)_{MNS}} \text{ and } \left(\frac{\left(\frac{W}{L}\right)_{MPS}}{2\left(\frac{W}{L}\right)_{MS2}} - \frac{1}{2} \right) = \left(\frac{\left(\frac{W}{L}\right)_{MNS}}{\left(\frac{W}{L}\right)_{MS3}} - 1 \right) = m \quad (11)$$

4. Design Example: full-wave current sensor with current output for a half-bridge automotive synchronous buck converter

This Section presents a design example for the current sensor described in the previous Section, that allows for a direct comparison with the sensor reported in [1]. For a fair comparison, the circuit shown in Fig. 5 was implemented in the same High-Voltage 180nm CMOS process, and sized for the same application as the one reported in [1]: full-wave current sensor with current output for a half-bridge synchronous buck converter. Moreover, have the same size as those used in [1].

a. Block diagram of the buck converter and main design requirements

The main design requirements for the automotive synchronous buck converter are summarized in TABLE I. Note the wide range of the supply voltage, from 6V to 45V, typical for automotive applications. The power switches M_P and M_N were set to the same sizes as those used in [1], hence the values of their drain-source resistances when turned fully on, listed in the last two rows of TABLE I.

The block diagram of the half-bridge synchronous buck converter considered here is similar to the one shown in Fig. 1.

Table 1. Design requirements for the Buck DC-DC Converter

Parameter	Value
Input voltage	6V to 45V
Nominal output voltage	5V
Output voltage ripple	<25mV
Maximum IL current	500mA
Switching frequency	500kHz
Rds_onMN	300mΩ
Rds_onMP	400mΩ

b. Design of a current-output sensor and simulation results

The compensation network and the external components of the buck converter were sized following the standard approach described in [6] and [12]. The resulting values for the inductor and output capacitance were $3\mu\text{H}$ and $10\mu\text{F}$, respectively.

The factor denoted K in Fig. 5 and in eqs. (9)-(11) was set to 1000, similar to the value used in [1]. Therefore, the Low-Side sense transistor, M_{NS} , has a width 1000 times smaller than the power switch M_N while the High-Side sense transistor M_{PS} , is 500 times smaller than the power switch M_P . The power switches and sense transistor have minimum length.

The biasing currents and the factor denoted m in eqs. (9)-(11) were sized considering the trade-off between the speed necessary to achieve the target accuracy while limiting the current consumption to 1mA: the bias current i_B was set to $120\mu\text{A}$, the current sources denoted I_1 and I_2 in Fig. 5 source $50\mu\text{A}$ each and the value of m was set to 5. The sensor designed here, with the top schematic shown in Fig. 5 and the transconductor schematics shown in Fig. 8, consumes just over 1mA, about 20% less than the sensor reported in [1].

The settling time and the GBW of the OpAmps formed by transconductor $Gm1$ and transistors $M2$, $M6$ and M_{PS} are: $t_{settle} = 71\text{ns}$ and $\text{GBW} = 22\text{MHz}$. The corresponding values for the OpAmp formed by $Gm2$, $M4$ and $M6$ are: $t_{settle} = 78\text{ns}$ and $\text{GBW} = 34\text{MHz}$. They are better than those indicated in [5] and [9], as a better accuracy is targeted here.

Fig. 9 presents simulation results obtained for the following conditions: 50% duty cycle for the signals that drive the power switches, named V_{GateHS} and V_{GateLS} in Fig. 7, and the inductor current varying between 300mA and 500mA (left) and 5mA and 250mA (right).

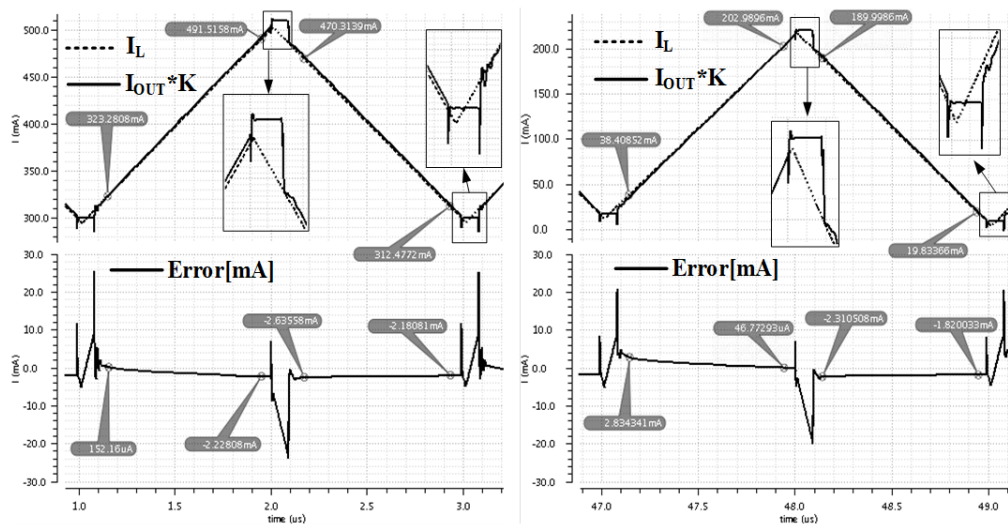


Fig. 9. Top: current outputted by the sensor shown in Fig. 5 scaled up and superimposed over the sensed current, I_L , that varies between 300mA and 500mA (left) and 5mA and 250mA (right), when the signals that control the power switches have a 50% duty cycle. Bottom: the absolute error, that is, the difference between the current yielded by the sensor multiplied by the factor K and the actual inductor current, I_L .

The top plots depict the current outputted by the sensor shown in Fig. 5 scaled up by the factor K and superimposed over the inductor current, I_L . The bottom plots show the absolute error, that is, the difference between the current yielded by the sensor and its ideal value. Fig. 10 and Fig. 11 present simulation results obtained for the same conditions, except for the duty cycle of the signals that drive the power switches, which was set to 10% and 80%, respectively.

The plots shown in Fig. 9 -Fig. 12 demonstrate that the sensor designed here is able to operate over the required wide range of input voltages and up to the maximum value of the inductor current listed in TABLE I. Furthermore, they also show that the absolute error during the sampling time intervals stays within (± 3 mA) for the 50% and 80% duty-cycle cases and within the interval (-2.5mA to +14.8mA) for the 10% duty-cycle case.

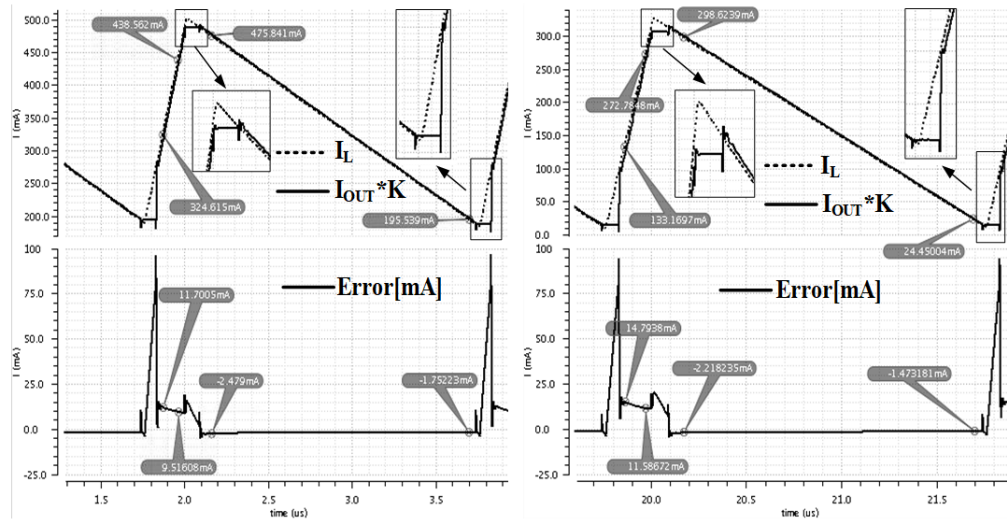


Fig. 10. Top: current outputted by the sensor shown in Fig. 5 scaled up and superimposed over the sensed current, I_L , that varies between 300mA and 500mA (left) and 5mA and 250mA (right), when the signals that control the power switches have a 10% duty cycle. Bottom: the absolute error, that is, the difference between the current yielded by the sensor multiplied by the factor K and the actual inductor current, I_L .

As expected, the error reaches large values during the Hold period, when the current sensor no longer tries to follow the inductor current but maintains its output at the level recorded just before the transition between High- and Low-Side conduction begins. The buck converter control circuitry is able to deal with this, as it sets the sensor in the Hold mode, and simply ignores the current sensor output during those time intervals. Furthermore, more sophisticated control systems can use interpolation to derive the extreme values of the inductor current, which occur during the Hold periods.

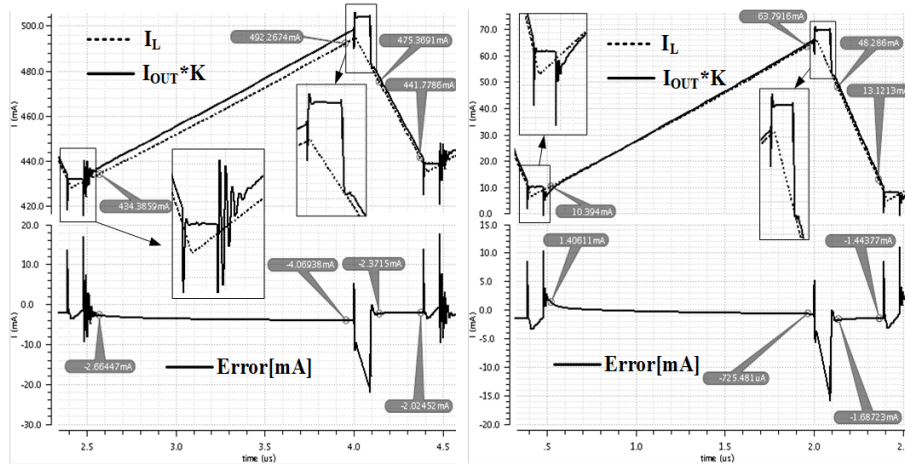


Fig. 11. Top: current outputted by the sensor shown in Fig. 5 scaled up and superimposed over the sensed current, I_L , that varies between 420mA and 500mA (left) and 5mA and 70mA (right), when the signals that control the power switches have an 80% duty cycle. Bottom: the absolute error, that is, the difference between the current yielded by the sensor multiplied by the factor K and the actual inductor current, I_L .

c. Design of a voltage-output sensor and simulation results

The voltage-output version presented in Fig. 6 was also implemented for this application. Fig. 12 presents simulation results obtained for the same conditions as the results depicted in Fig. 9: 50% duty cycle for the signals that drive the power switches and the inductor current varying between 300mA and 500mA (left) and 5mA and 250mA (right).

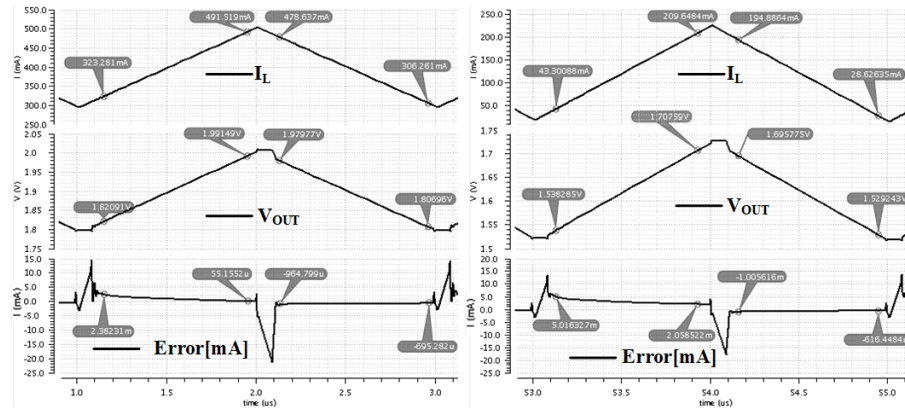


Fig. 12. Top: the sensed current, I_L , that varies between 300mA and 500mA (left) and 5mA and 250mA (right). The signals that control the power switches have a 50% duty cycle. Middle: the output voltage yielded by the sensor shown in Fig. 6. Bottom: the absolute error, that is, the difference between the current indicated by the sensor - derived from its output voltage by using eq. (7) and the actual value, I_L .

By comparing results shown in Fig. 9 and Fig. 12 one notices that the current-output current sensor and its voltage-output version yielded similar peak-to-peak absolute error, considering only the sampling time intervals: 5.5mApkpk and 5.7mApkpk, respectively.

d. Comparative analysis of sensor range and accuracy

Let us compare the performance of the current sensor proposed in this work, described in the previous Section, against the performance of two similar sensors reported in [1] and [3]. To extend the range of this comparison we also designed an own version of the sensor reported in [2], by using the same process and targeting the same requirements as the sensor presented here and the one reported in [1].

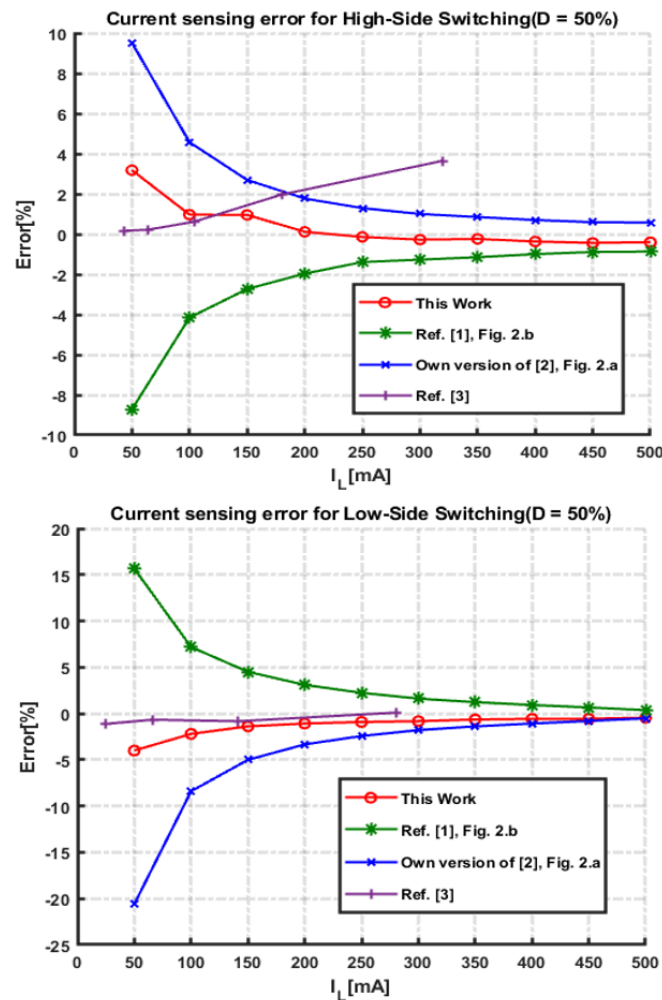


Fig. 13. The relative error as a function of the sensed current, I_L , in High-Side (top) and Low-Side (bottom) modes, when the signals that drive the power switches have a 50% duty cycle, for four sensors: the one proposed here (circle marks), the ones reported in [1] (star) and [3] (vertical marks), and an own version of the sensor reported in [2] (cross).

Fig. 13 presents the relative error of the four sensors mentioned above as a function of the sensed current, I_L , when the signals that drive the power switches have a 50% duty cycle and the sensor operates in High-Side (top) and Low-Side (bottom) modes.

The sensor proposed here, described in the previous Section (plots with circle marks) exhibits the best overall performance: its error is always smaller than for the sensor reported in [1] (star marks) and for the own version of the sensor reported in [2] (cross marks); the sensor reported in [3] (vertical marks) has a smaller error for I_L values up to 120mA but its error increases as the value of I_L increases, reaching 2% for $I_L = 180$ mA; also, it cannot handle inductor currents larger than 320mA.

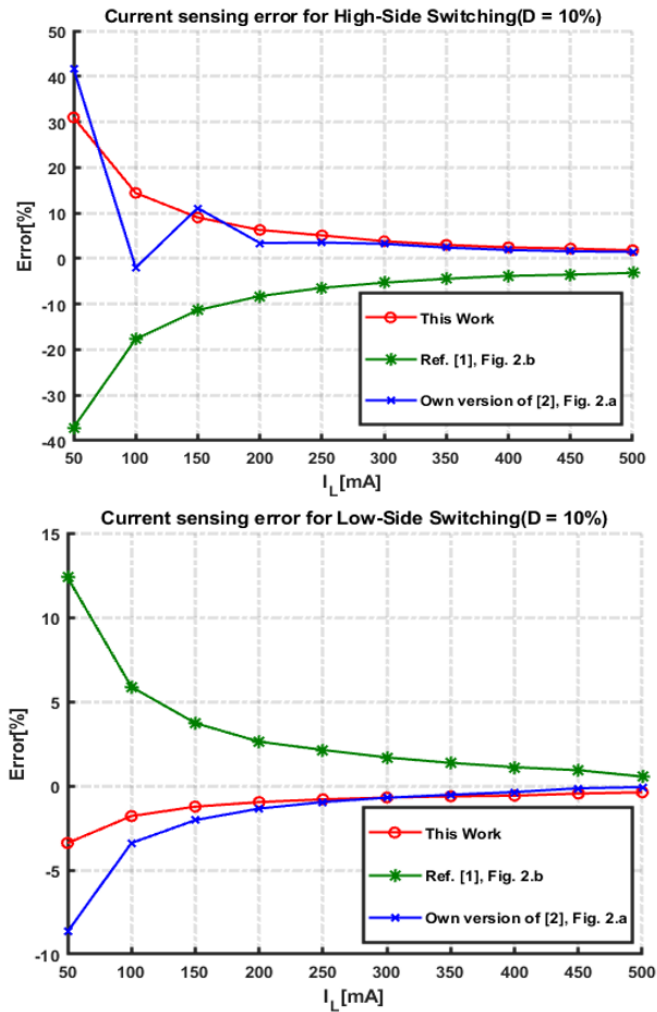


Fig. 14. The relative error as a function of the sensed current, I_L , for the sensor proposed here, shown in in Fig. 5 (circle marks), the one reported in [1] (star) and the one reported in [2] designed in the same process as the other two (cross). The signals that drive the power switches have a 10% duty cycle, and the sensors operate in High-Side (top) and Low-Side (bottom) modes.

Fig. 14 and Fig. 15 present simulation results obtained for the same conditions, except for the duty cycle of the signals that drive the power switches, which was set to 10% and 80%, respectively. No data are available for the sensor reported in [3] for these cases.

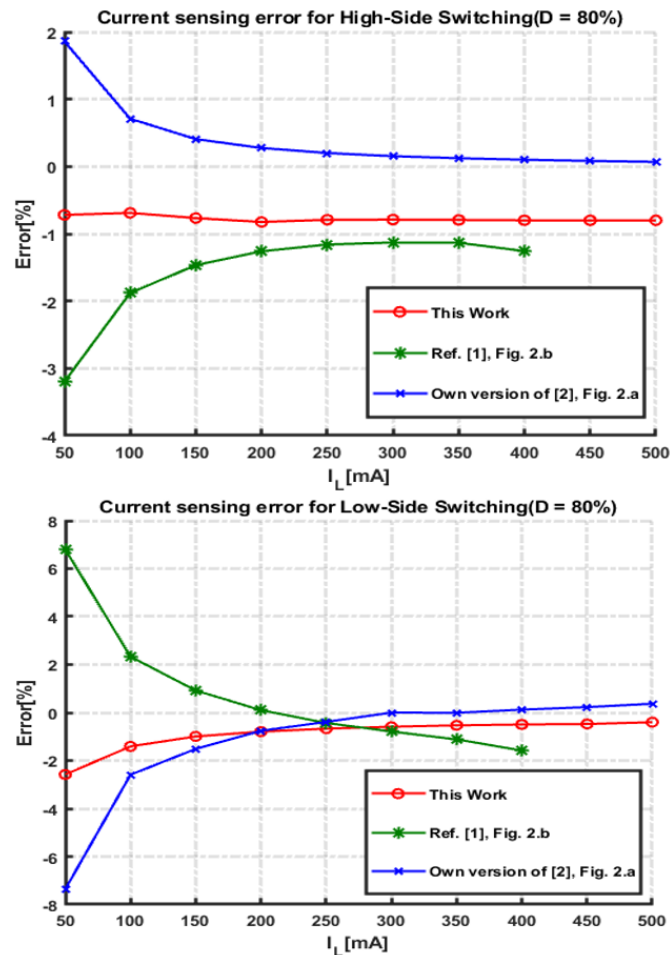


Fig. 15. The relative error as a function of the sensed current, I_L , for the sensor proposed here, shown in in Fig. 5 (circle marks), the one reported in [1] (star) and the one reported in [2] designed in the same process as the other two (cross). The signals that drive the power switches have a 10% duty cycle, and the sensors operate in High-Side (top) and Low-Side (bottom) modes.

The sensor proposed here, with the top schematic shown in Fig. 5 and the transconductors implemented as shown in Fig. 8, yields smaller errors than the one reported in [1] for all I_L values, for both extreme duty-cycle values. For the 10% duty-cycle case, it also has a better overall performance than the own version of the sensor reported in [2] (designed in the same process and to the same requirements as the other two sensors). For the 80% duty-cycle case and I_L values above 120mA, its error is slightly larger than the one yielded by the own version of the sensor reported in [2], but the error values are smaller than 1

5. Conclusions

A novel topology for full-wave current sensors based on the V_{ds} -sense technique, suitable for synchronous buck converters, was presented along with effective circuit implementations. The novel sensor was derived by addressing the main limitations of a solution published previously by the same authors. Both the circuit topology and circuit implementation were improved in order to increase the sensor accuracy and make it better suited to the wide range of input voltages required by automotive applications.

The two main topology improvements were: i). the Sample&Hold circuit, used to prevent large signal spikes to appear at the output during transitions between the High- and Low-side operation modes, was embedded in a new output stage and ii). a high-voltage transistor was placed between the High-Side sense transistor and the main current mirror, so that it not only insulates the current mirror from the large supply voltage but also implements a gain stage in the High-Side sense signal path. Thus, the new topology allows for most of the signal paths, including the active elements, to be implemented by using low-voltage transistors. Furthermore, the active elements do not need to provide large gains and to drive large loads, so they can be implemented by one-stage transconductors. Finally, the topology allows for a simple, two-steps trimming procedure, that can reduce significantly the effect of mismatches inherent to an integrated implementation.

The paper presented compact and power-efficient circuit implementations for the High- and Low-Side transconductors, based on the common-gate topology. Effective circuit solutions for the output stage and the Sample&Hold circuit were also proposed.

The advantages of the novel full-wave current sensor were highlighted by a design example: a synchronous buck converter for automotive applications designed in a 180nm High-Voltage CMOS process. The sensor had to monitor currents from 500mA down to 50mA while the input voltage ranged between 6V and 45V, which resulted in a wide range of duty-cycle values for the signals that drove the power switches – between 10% and 80%. Simulation results presented in the paper validated the design and demonstrated the effectiveness of the improvements described above. The novel sensor yielded significantly smaller errors than the one previously reported by the authors, for all values of the sensed current, over the entire duty-cycle range.

The sensor proposed here was also compared against two other sensors published previously that operate under similar conditions. Overall, the proposed sensor performs better than its counterparts on several counts:

- relative error under 1.2% peak-to-peak for inductor currents larger than 200mA and below 7.2% peak-to-peak down to 50mA, when the signals that drive the power switches have a 50% duty cycle;
- the error decreases as the inductor current increases: relative peak-to-peak error over the entire range of duty-cycle values, 10% to 80%, decreases from just under 10% for inductor currents larger than 150mA, to better than 7.2% for currents above 200mA and to only 4.5% for inductor currents larger than 300mA.

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