

## New Constant-gm circuit for precision chopper offset-stabilized operational amplifiers

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**Abstract.** The paper presents a low-voltage chopper offset-stabilized operational amplifier with a new constant-gm technique, having a 1.8–5.5 V supply range, designed and simulated in a 0.25  $\mu\text{m}$  CMOS process. The amplifier has an offset voltage of  $\pm 5 \mu\text{V}$ , minimum CMRR of 106 dB, minimum PSRR of 121 dB, 51  $\text{nV}/\sqrt{\text{Hz}}$  voltage noise density and 550 kHz unity-gain bandwidth. The quiescent current is only 36  $\mu\text{A}$  and was obtained due to the new low current constant-gm technique, which provides a variation of only 4% of the input transconductance and almost constant unity-gain bandwidth within the common-mode voltage range.

**Key-words:** Microelectronics and electronic packaging, chopper offset-stabilized operational amplifier, constant-gm, low current, offset voltage, noise.

### 1. Introduction

This paper is an extended version of [1] and presents a chopper offset-stabilized operational amplifier that uses a new constant-gm technique. The operational amplifier has a 1.8–5.5 V supply range and was realized in a 0.25  $\mu\text{m}$  CMOS process.

A current trend in operational amplifiers design is lowering the supply voltage. A low supply voltage often results in a reduced input common-mode range. Because of this, it is important that operational amplifiers have rail-to-rail input stages. This ensures maximum use of the voltage range between the negative and positive supply rails.

Most commonly, rail-to-rail input stage use complementary differential pairs operated in parallel. Unfortunately, the transconductance of this input stage decreases by half when the

common-mode voltage is close to supply voltage rails. A variable transconductance causes a variable unity-gain frequency. Thus, stability problems can result [2].

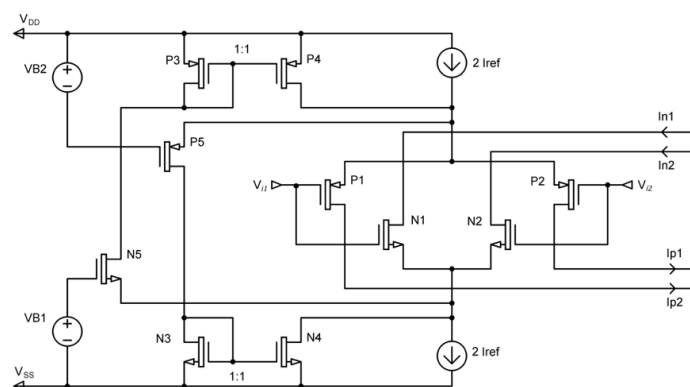
The first part of the paper will present several related-art constant-gm techniques. Based on them, a new constant-gm architecture was developed and will be presented in the second part of the paper. To prove its benefits, the proposed constant-gm technique was integrated in a chopper offset-stabilized operational amplifier. The amplifier topology, schematic and simulations will be presented in the last part of the paper.

## 2. Constant-gm techniques

This chapter will present several known constant-gm architectures that were a starting point for the development of a new, more efficient architecture. To explain the working principle of related-art techniques it will be considered that input stages are operated in weak inversion for maximum transconductance at a given current. That being said, to maintain the transconductance constant over the entire common-mode input voltage range, it is necessary to maintain constant the sum of the tail currents.

The first related-art, called “Constant-gm by Constant Sum of Tail-Currents”, is described in [2, 3] and shown in Fig. 1. When common-mode voltage ( $V_{CM}$ ) is in the middle, both nMOS and pMOS input differential pairs have proper operating point (OP) making the tail-currents of both input pairs being equal with  $2I_{REF}$ . When common-mode voltage is low or high, close to one supply rail, only one pair operates. The current-switches N5 and P5, and the 1:1 current mirrors N3-N4 and P3-P4, are increasing the tail-current of the active input pair by a factor of 2 by adding the tail current of the inactive pair. Thus, the tail-current of the actual active input pair has a value of  $4I_{REF}$  and the total input stage transconductance remains constant.

This technique has the advantage of zero supplementary current consumption when  $V_{CM}$  is in the middle. The downside is that the current consumption of the circuit increases with  $2I_{REF}$  when  $V_{CM}$  is close or above supply rails (a branch of  $2I_{REF}$  is added due to 1:1 current mirrors, Fig. 1). This is unacceptable in applications where current consumption is a critical parameter.



**Fig. 1.** Rail-to-rail CMOS input stage with 1:1 current mirrors.

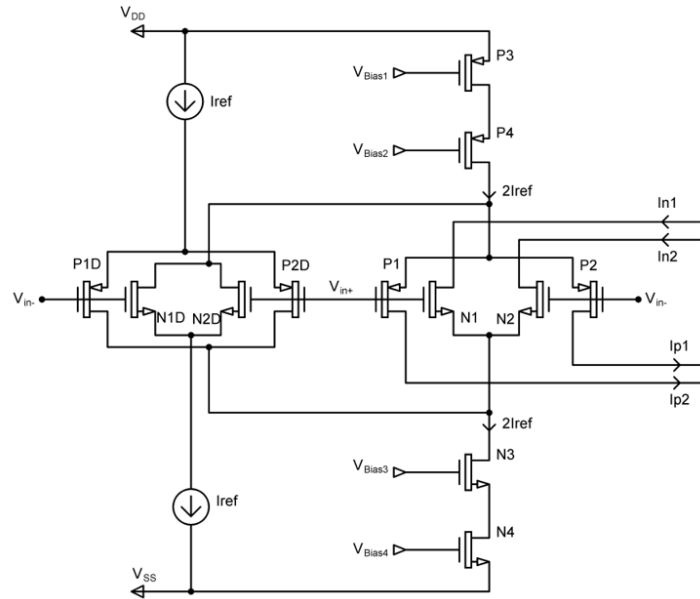
The second related art is known as “Constant-gm in CMOS by Saturation Control” and is described in [4] and [5]. Fig. 2 shows the circuit used. To achieve a constant transconductance over the input common-mode ( $V_{CM}$ ) range, dummy differential pairs are used (N1D, N2D, P1D,

P2D). The working principle is described by dividing the input common-mode voltage range in three regions.

Region I analysis implies low common-mode voltage, when  $V_{CM} < V_{DD} - 2V_{SDP,sat} - V_{SG}$ . In this region, only the pMOS main differential pair (P1, P2) and the pMOS dummy pair (P1D, P2D) work. The other two nMOS pairs are in the cut-off region and no current flows through them. Then  $I_{ref}$  current flows through each of P1 and P2. The total transconductance in region I is expressed as:

$$g_{mT,I} = g_{mP} = \frac{I_{ref}}{n_P V_{th}} = \frac{I_{ref}}{n V_{th}} \quad (1)$$

where  $V_{th}$  is the thermal voltage and  $n_P$  is the subthreshold slope factor for pMOS input transistors. For simplicity, let  $n_N = n_P = n$ .



**Fig. 2.** Constant-gm in CMOS by Saturation Control.

When common mode voltage is in the middle range (region II:  $V_{SS} + 2V_{DSN,sat} + V_{GS} < V_{CM} < V_{DD} - 2V_{SDP,sat} - V_{SG}$ ), both pMOS and nMOS differential pairs are turned on. The total transconductance is:

$$g_{mT,II} = g_{mN} + g_{mP} = \frac{I_{ref}}{2n_N V_{th}} + \frac{I_{ref}}{2n_P V_{th}} = \frac{I_{ref}}{n V_{th}} \quad (2)$$

Region III defines high common-mode voltage operation:  $V_{CM} > V_{SS} + 2V_{DSN,sat} + V_{GS}$ . Only the nMOS main pair (N1 and N2) and the nMOS dummy pair (N1D and N2D) work. pMOS differential pairs are in the turn-off region.  $I_{ref}$  current flows through each of N1 and N2. The total transconductance in region III is:

$$g_{mT,III} = g_{mN} = \frac{I_{ref}}{n_N V_{th}} = \frac{I_{ref}}{n V_{th}} \quad (3)$$

The total transconductance remains the same by doubling the tail current of the active differential pair when the other differential pair shuts off. The current consumption of this circuit (including the additional currents that are sourced/sunk from/into the following stage) is the same over entire  $V_{CM}$  domain. Thus, the main disadvantage of this method to obtain constant-gm (Fig. 2) is the significant additional current ( $2I_{ref}$ ).

Moreover, both related-art architectures have the downside of double DC output currents of the differential pairs ( $I_{n1}$ ,  $I_{n2}$ , and  $I_{p1}$ ,  $I_{p2}$ ) in regions I and III of the common-mode voltage. This may cause improper operation of the following gain stage. Several other methods to ensure constant gm are available in related art, but they are not suitable for precision operational amplifiers, [6] being an example.

### 3. Proposed Constant-gm Technique

The proposed constant-gm technique maintains the input stage transconductance constant, while reducing the current consumption compared to the other two presented techniques.(Fig. 1 and Fig. 2).

Fig. 3 shows the proposed circuit schematic. As the second classical approach, this method also uses dummy differential pairs. Current mirrors are used to supply additional current to the main differential pairs. The same three regions for common-mode voltage are used to describe the working principle. The main differential pairs use low voltage threshold (LVT) transistors to cope with the minimum supply voltage of 1.8 V of the operational amplifier in which the circuit will be used.

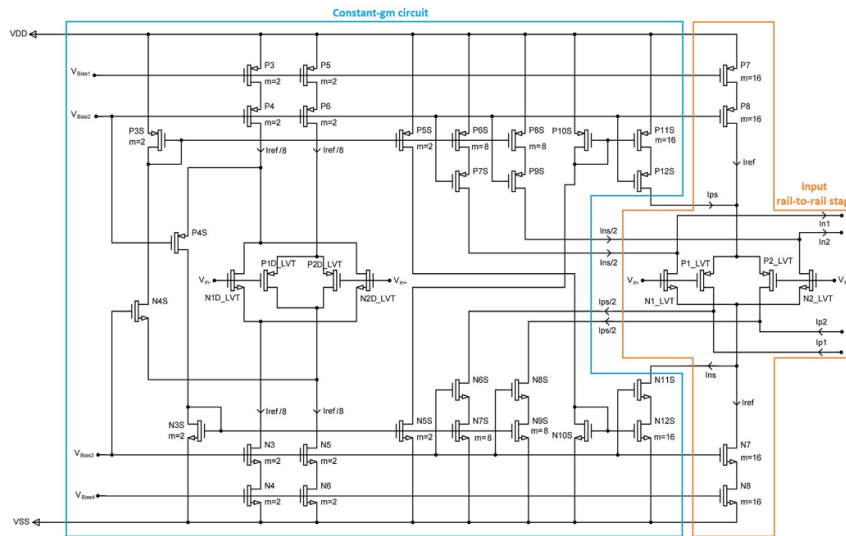


Fig. 3. Schematic of the rail-to-rail input stage with proposed constant-gm circuit.

When common-mode voltage is low (region I) only the pMOS differential pairs are turned on. Because N1D and N2D are off, the current generated by the mirror consisting of P3 and P4 ( $I_{ref}/8$ ) flows through P4S (Fig. 3). It is then mirrored by N3S, N5S and P10S, multiplied 8 times by mirror P11S and P12S and inserted in the main pMOS pair.  $I_{ps}$  is now equal to  $I_{ref}$ .

$2I_{ref}$  current flows through each of  $P1\_LVT$  and  $P2\_LVT$ . Thus total transconductance is same as (1).

In order to maintain output currents of the pMOS pair ( $P1\_LVT$  and  $P2\_LVT$ )  $I_{p1} = I_{p2} = I_{ref}/2$ , current mirrors consisting of N6S through N9S were added to subtract the additional current  $I_{ps}$  (Fig. 3).

Region II defines the middle of the common-mode voltage range. Both pMOS and nMOS pairs are turned on. Current flows from P mirrors (P3 through P6) to N mirrors (N3 through N6).  $I_{ps}$  and  $I_{ns}$  are zero in this region. Total transconductance is described by (2).

In the third region, the common voltage is high. The working principle of the input stage is similar to the one described in the first region, but this time the pmos transistors are off, while the nmos pairs are on. N11S and N12S insert an additional current in the main nmos differential pair, so a current twice the value of  $I_{ref}$  flows. Total transconductance is same as (3). Current mirrors consisting of P6S through P9S subtract the additional current,  $I_{ns}$ . Thus,  $I_{n1}$  and  $I_{n2}$  maintain their  $I_{ref}/2$  value.

The proposed technique uses significantly lower current than second related-art when the common-mode voltage is in the middle region. Only  $I_{ref}/4$  is consumed by the constant-gm circuit. Also, comparing with first related-art, only  $I_{ref}/8$  is added when common-mode voltage is low or high (due to current mirrors). The reference current ( $I_{ref}$ ) can be optimized by choosing the right W/L ratio of the current mirrors that bias the dummy differential pairs.

Also, another advantage is that the DC output currents of the main differential pairs ( $I_{n1}, I_{n2}$  and  $I_{p1}, I_{p2}$ ) are kept constant over  $V_{CM}$ . Thus, the following stage is not influenced by the constant-gm circuitry.

The proposed circuit has also some limitations. Due to additional current mirrors, the circuit is slower than the two related-arts described above. Also, the circuit has a higher grade of complexity.

Fig. 4 shows the performances of the proposed constant-gm circuit depicted in Fig. 3. The graph plots the pMOS and nMOS main differential pairs transconductances, as well as the total transconductance, both versus  $V_{CM}$ . The values are normalized. Simulation was performed at a supply voltage of 3.3 V, at room temperature.  $I_{ref}$  was chosen  $16 \mu A$ . Input transistors were dimensioned to operate in weak inversion at  $I_{ref}$ .

Total simulated transconductance varies by only 4% within entire common-mode voltage range (from  $V_{SS} - 100 mV$  to  $V_{DD} + 100 mV$ ).

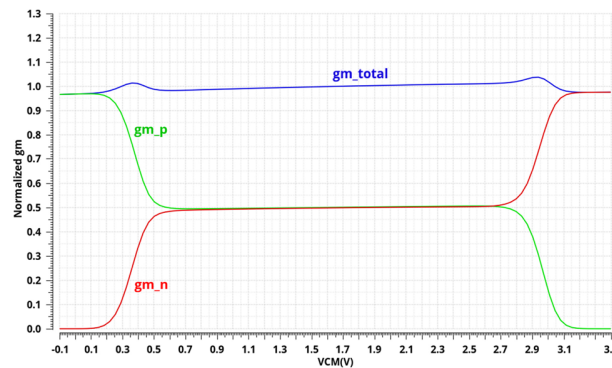
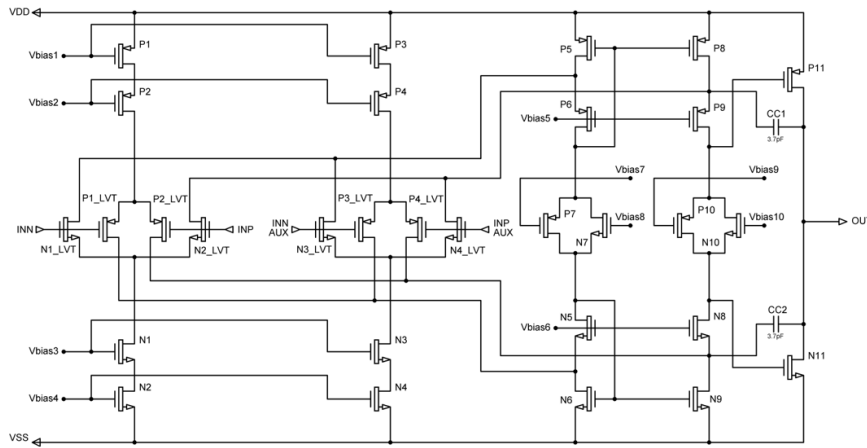


Fig. 4. Proposed constant-gm circuit - input gm vs.  $V_{CM}$ .

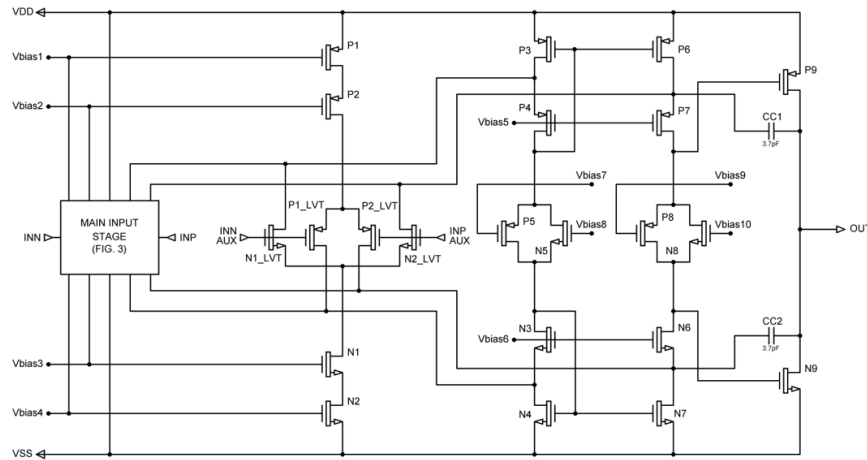


architecture [12]-[14] is used for the output stage. The amplifier is frequency compensated by CC1 and CC2, in a cascoded Miller classical architecture.

Fig. 7 presents the main amplifier schematic including constant-gm technique. The “Main input stage” block contains the schematic showed in Fig. 3, which includes the input stage and constant-gm circuit.



**Fig. 6.** Main amplifier without constant-gm – schematic.



**Fig. 7.** Main amplifier with constant-gm - schematic.

Further, simulations with the main amplifier will be presented. Fig. 8 and Fig. 9 show the frequency response of the main amplifier without and with constant-gm architecture. Table 1 summarize UGBW (Unity-Gain Bandwidth) and PM (Phase Margin) results. Also, the IQ (Quiescent Current) vs.  $V_{CM}$  simulation results were added. At middle  $V_{CM}$ , unity-gain frequency is 576 kHz with 58° phase margin. Without constant-gm, the unity-gain frequency drops to 300 kHz at high or low  $V_{CM}$  (Fig. 8). Due to constant-gm circuit (Fig. 9), unity-gain frequency is almost constant (minimum of 556 kHz).

At middle  $V_{CM}$ , the constant-gm circuit has a current consumption of only  $0.41 \mu\text{A}$  (IQ rises from  $21.84 \mu\text{A}$  to  $22.21 \mu\text{A}$ ). Also, in the third chapter it was documented that only  $I_{ref}/8$  is added when common-mode voltage is low or high. Due to low current constant-gm circuit and variation of the output stage bias current versus  $V_{CM}$ , IQ at low or high  $V_{CM}$  is even smaller than the one for middle common-mode voltages (Table 1).

Simulations were performed at a differential supply voltage of  $\pm 1.65 \text{ V}$ , for  $V_{CM}$  of  $-1.55 \text{ V}$ ,  $0$  and  $1.55 \text{ V}$ , at room temperature. The auxiliary inputs were shorted and connected to a proper, stable  $V_{CM}$ . The amplifier stability cannot be simulated over the whole  $V_{CM}$  range (from  $V_{SS} - 100 \text{ mV}$  to  $V_{DD} + 100 \text{ mV}$ ) because the output voltage range is limited by the output stage transistors drain-source voltages  $V_{DS}$  in saturation. Therefore, the  $V_{CM}$  range was chosen at  $100 \text{ mV}$  within the supply rails.

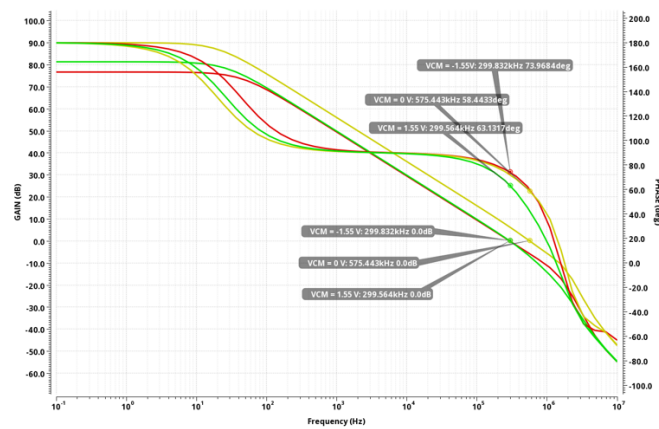


Fig. 8. Closed-loop frequency response of the main amplifier without constant-gm.

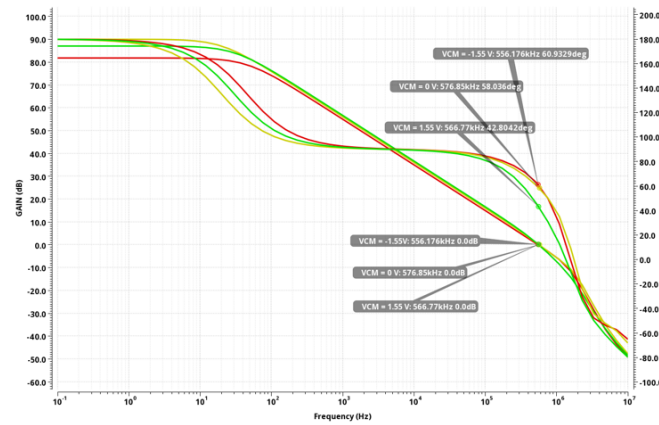


Fig. 9. Closed-loop frequency response of the main amplifier with constant-gm.

**Table 1.** Main amplifier performances vs.  $V_{CM}$  ( $V_S = \pm 1.65$  V)

Main amplifier without constant-gm (Fig. 6)					
$V_{CM}$ [V]	-1.75	-1.55	0	1.55	+1.75
UGBW [kHz]	-	299.8	575.4	299.6	-
PM [°]	-	73.9	53.4	63.1	-
$I_Q$ [ $\mu$ A]	17.43	17.44	21.84	16.73	16.71
Main amplifier with constant-gm (Fig. 7)					
UGBW [kHz]	-	556.2	576.9	566.8	-
PM [°]	-	60.9	58	42.8	-
$I_Q$ [ $\mu$ A]	20.21	20.22	22.25	19.63	19.62

CMRR and offset voltage ( $V_{OS}$ ) of the main amplifier were simulated (Table 2). The addition of the constant-gm circuit reduced the  $V_{OS}$  with around 0.5 mV and increased the minimum CMRR with 2 dB. These improvements are validating the proposed constant-gm circuit. Results are obtained from Monte Carlo simulation with 100 runs at a differential supply voltage of  $\pm 1.65$  V.

**Table 2.** Main amplifier performances vs.  $V_{CM}$  ( $V_S = \pm 1.65$  V)

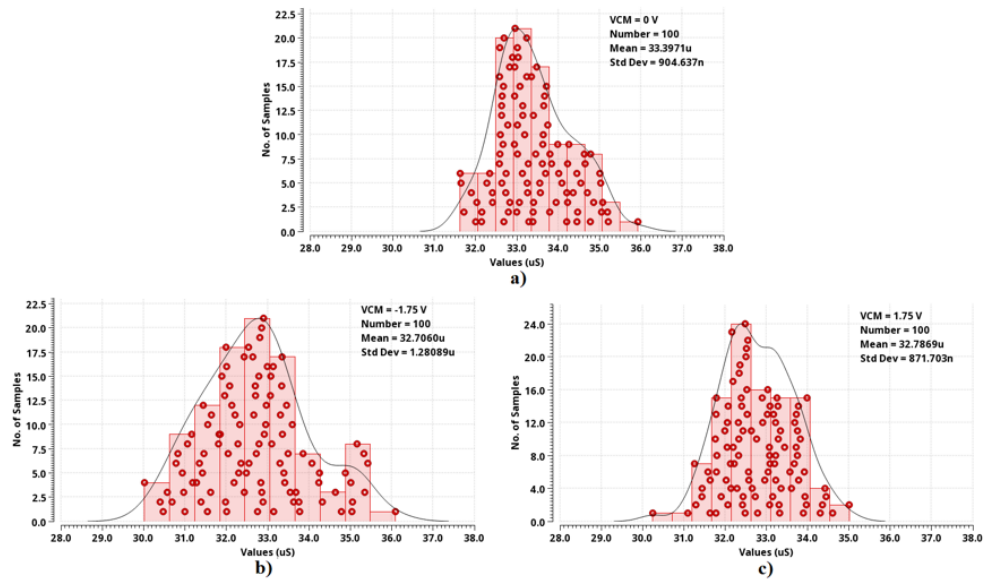
Param.	Temp. [°C]	Main amplifier without constant-gm (Fig. 6)			
		Min.	Max.	Mean ( $\mu$ )	Std. Dev. ( $\sigma$ )
$V_{OS}$ [mV]	-40	-2.485	3.032	0.071	0.988
	25	-2.524	3.078	0.068	1.003
	125	-2.579	3.134	0.060	1.022
CMRR [dB]	-40	58.2	110.2	73.71	9.34
	25	58.17	119.5	73.79	9.847
	125	58.1	101	73.51	8.913
Main amplifier with constant-gm (Fig. 7)					
$V_{OS}$ [mV]	-40	-1.971	2.472	0.053	0.925
	25	-2.044	2.485	0.051	0.939
	125	-2.154	2.495	0.045	0.960
CMRR [dB]	-40	60.30	101.50	72.79	9.31
	25	60.07	116.40	72.85	9.91
	125	59.7	100.7	72.46	9.21

Also, in order to prove the constant-gm circuit performances, a Monte Carlo analysis in 300 points was performed to see the process variation of the input transconductance vs.  $V_{CM}$ . Fig. 10 shows the obtained histograms. The constant gm technique shows great performance with process variation, the transconductance having a maximum standard deviation of only  $1.08 \mu$ S. Simulation was performed at  $\pm 1.65$  V supply voltage, room temperature and  $V_{CM}$  of 0 V, -1.75 V and 1.75 V.

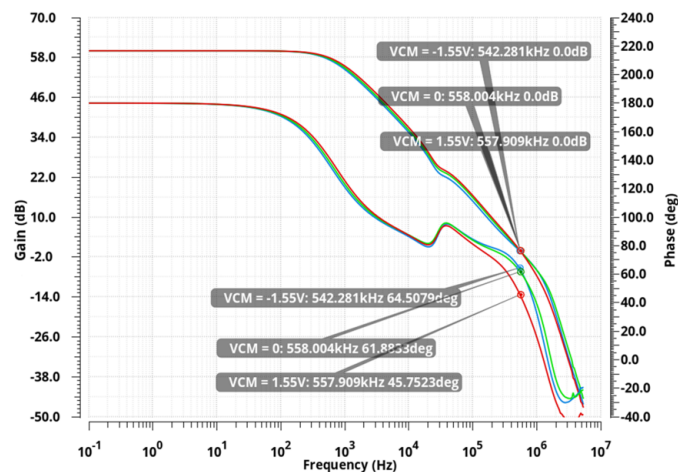
Results shown so far were related to the constant-gm architecture and its performances. Further, simulations with the chopper offset-stabilized amplifier (Fig. 5) will be shown. The following parameters (such as offset voltage, voltage noise density, slew rate, settling time) will be presented in order to see advantages and disadvantages of chopper offset-stabilization technique. The proposed constant-gm circuit was used for the input stage of the main amplifier (Fig. 7) as well as for the input stage of null amplifier.

Fig. 11 shows the stability diagram of the chopper offset-stabilized operational amplifier for  $V_{CM}$  of -1.55 V, 0 and 1.55 V, at room temperature. Comparing it with the graph shown in Fig.

9, it can be seen that the chopper offset-stabilization has a quite bad influence on gain and phase evolution in frequency, due to the new added signal path. The unity-gain frequency is 558 kHz, slightly smaller than the one of the main amplifier, because of the nested Miller capacitors. The constant-gm circuit main advantage is also proven: the unity-gain frequency is almost constant at low or high  $V_{CM}$ . Minimum phase margin is 45.75° at  $V_{CM} = 1.55$  V. The amplifier stability was simulated in a non-inverting configuration, with the gain set to 60 dB, a differential supply voltage of  $\pm 1.65$  V, at room temperature.



**Fig. 10.** Main amplifier input transconductance at a)  $V_{CM} = 0$  V, b)  $V_{CM} = -1.75$  V and c)  $V_{CM} = 1.75$  V.



**Fig. 11.** Closed-loop frequency response of the chopper offset-stabilized amplifier.

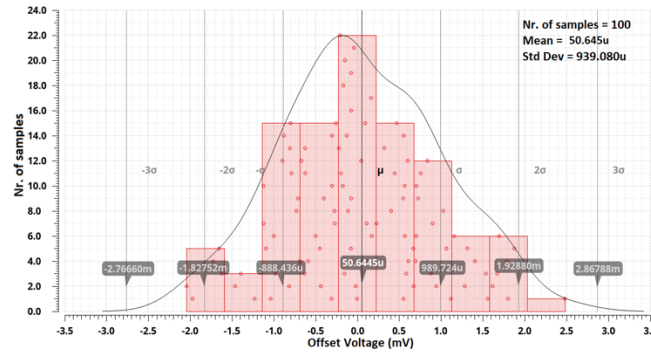
Table 3 summarize UGBW, PM and IQ vs  $V_{CM}$  results. Comparing with the main amplifier IQ (Table 1), quiescent current of the chopper amplifier is slightly higher at lower  $V_{CM}$  as against middle  $V_{CM}$ .

**Table 3.** Chopper amplifier performances vs.  $V_{CM}$  ( $V_S = \pm 1.65$  V)

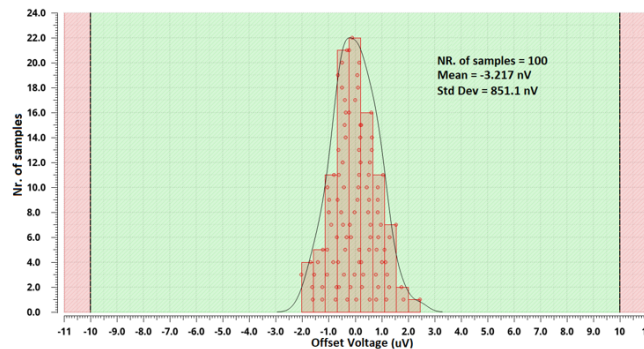
$V_{CM}$ [V]	-1.75	-1.55	0	1.55	+1.75
UGBW [kHz]	-	542.3	558.0	557.9	-
PM [°]	-	54.5	61.9	45.8	-
$I_Q$ [ $\mu$ A]	36.42	36.38	35.9	33.89	33.91

Fig. 12 and Fig. 13 shows the main amplifier with constant-gm (Fig. 7) and chopper offset-stabilized amplifier (Fig. 5) offset voltage distribution. An average offset voltage of  $50.6 \mu$ V and a standard deviation of  $939 \mu$ V were obtained for main amplifier (Fig. 12). The obtained value for the offset voltage is quite good for an operational amplifier with IQ of only  $22 \mu$ A that does not have offset-stabilization.

In Fig. 13 the chopper offset-stabilization advantages can be seen. The main amplifier offset is reduced by the chopper offset-stabilization loop with three orders of magnitude. Note that main amplifier has the schematic shown in Fig. 7. Monte Carlo simulation was carried out at 3.3 V overall supply voltage, room temperature and 100 runs.



**Fig. 12.** Main amplifier with constant-gm - offset voltage.



**Fig. 13.** Chopper offset-stabilized amplifier - offset voltage. Limit of  $\pm 10 \mu$ V (maximum required offset voltage) are applied.

The next important parameter improved by chopper-offset stabilization is the input voltage noise density. Fig. 14 shows the input voltage noise density of the main amplifier with constant-gm. The classical shape of 1/f noise can be observed; a voltage noise density of  $1.65 \mu\text{V}/\sqrt{\text{Hz}}$  was simulated at 1 Hz. In Fig. 15 it can be seen that the 1/f frequency noise has been completely removed by chopper-stabilization, the noise density being flat down to 0.1 Hz with a value of  $50.13 \text{ nV}/\sqrt{\text{Hz}}$ .

Unfortunately, chopper offset-stabilization has also some drawbacks. Fig. 17 present the settling time of the chopper offset-stabilized amplifier which was increased from  $3.2 \mu\text{s}$  (for the main amplifier with constant-gm – Fig. 16) to  $57.5 \mu\text{s}$ . Values are obtained for unity-gain configuration.

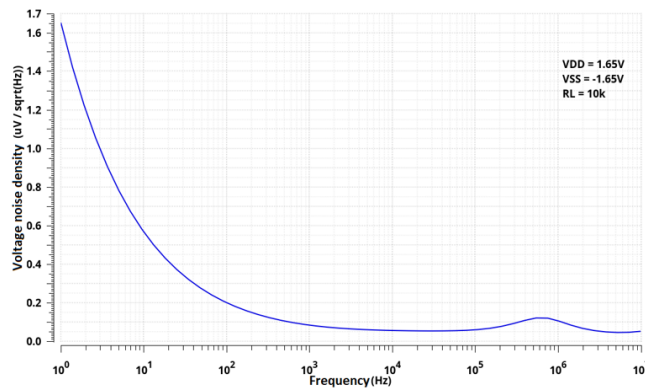


Fig. 14. Main amplifier with constant-gm - input voltage noise density.

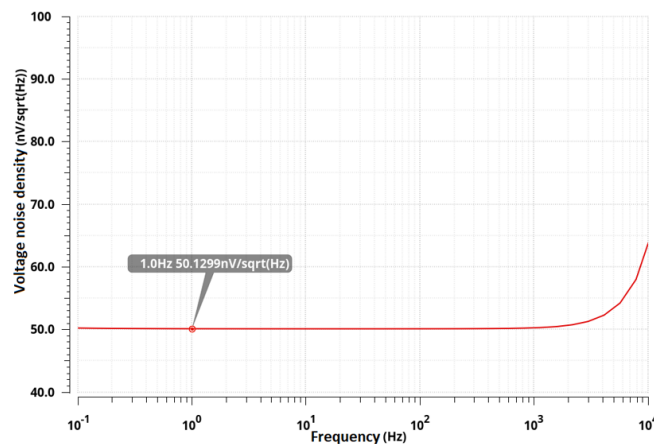


Fig. 15. Chopper offset-stabilized amplifier - voltage noise density.

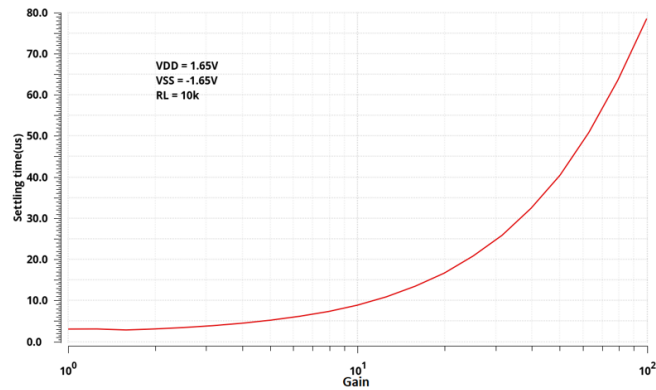


Fig. 16. Main amplifier with constant-gm - settling time to 0.1%.

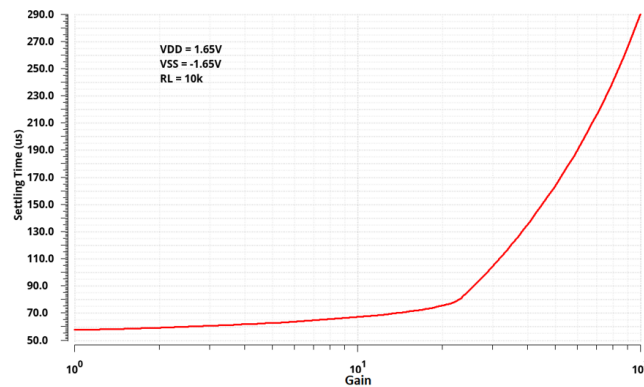


Fig. 17. Chopper offset-stabilized amplifier – settling time to 0.1%.

Chopper offset-stabilization also worsens the slew rate and the step response. Slew rate decreases from 1.1 V/ $\mu$ s (Fig. 18) to 0.36 V/ $\mu$ s (Fig. 19). Smaller slew rate and bigger settling time lead to a worse step response of the chopper offset-stabilized amplifier (Fig. 21) as against the main amplifier (Fig. 20).

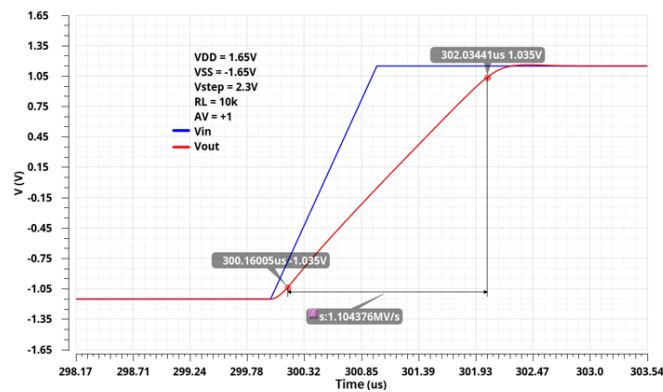


Fig. 18. Main amplifier with constant-gm – slew rate.

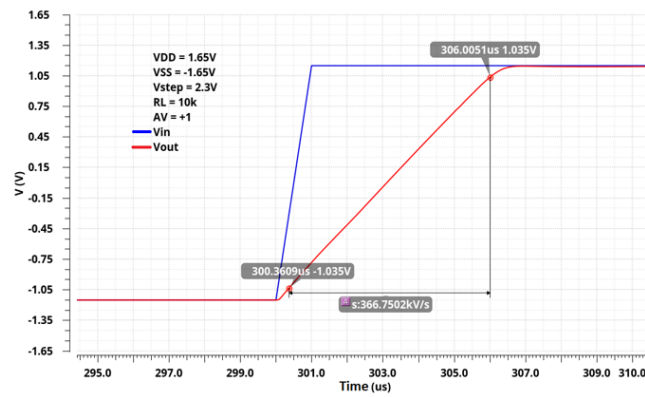


Fig. 19. Chopper offset-stabilized amplifier – slew rate.

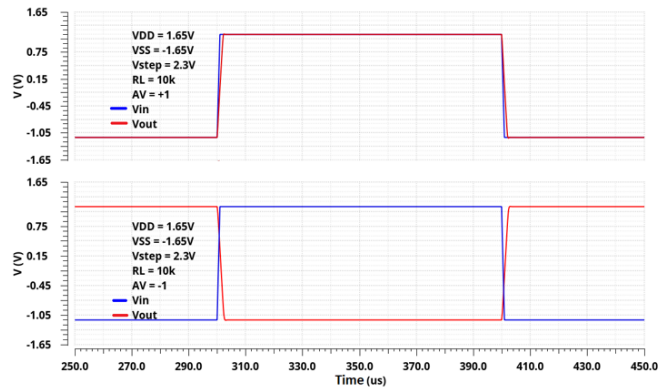


Fig. 20. Main amplifier with constant-gm – large step response.

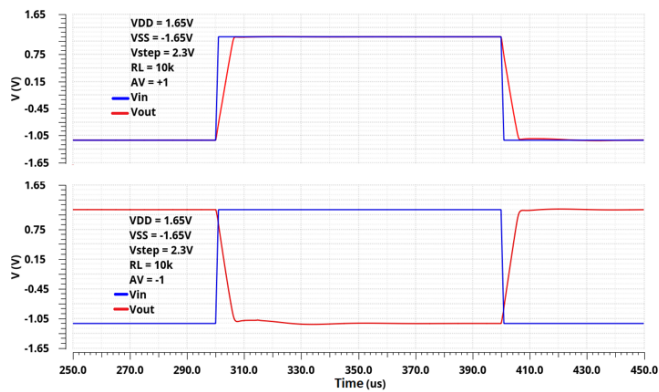


Fig. 21. Chopper offset-stabilized amplifier – large step response.

Table 4 presents the PVT results of chopper offset-stabilized amplifier (Fig. 5) regarding input precision, by means of offset voltage and offset voltage drift in temperature (Monte Carlo simulation with 100 runs). Offset voltage value is between  $-4.2 \mu\text{V}$  and  $4.9 \mu\text{V}$ . From this point of view, the chopper offset-stabilization technique brought a sizeable improvement.

**Table 4.** Chopper offset-stabilized amplifier - offset voltage and offset voltage drift vs. temperature and process variation.

Param	Temp. [ $^{\circ}\text{C}$ ]	$V_{DD}=0.9\text{ V}, V_{SS}=-0.9\text{ V}$			
		Min.	Max.	Mean ( $\mu$ )	Std. Dev. ( $\sigma$ )
$V_{OS} [\mu\text{V}]$	-40	-3.239	2.54	-0.029	0.998
	25	-2.732	3.065	0.032	1.009
	125	-3.287	4.393	0.056	1.387
$\Delta V_{OS}/\Delta T [\text{nV}/^{\circ}\text{C}]$		-21.07	11.23	0.519	5.224
		$V_{DD}=1.65\text{ V}, V_{SS}=-1.65\text{ V}$			
$V_{OS} [\mu\text{V}]$	-40	-1.847	4.168	0.036	0.873
	25	-2.033	2.45	-0.003	0.851
	125	-3.067	3.6	0.038	1.227
$\Delta V_{OS}/\Delta T [\text{nV}/^{\circ}\text{C}]$		-23.64	11.18	0.010	5.127
		$V_{DD}=2.75\text{ V}, V_{SS}=-2.75\text{ V}$			
$V_{OS} [\mu\text{V}]$	-40	-2.679	2.922	0.061	1.216
	25	-3.426	4.038	-0.036	1.46
	125	-4.199	4.896	-0.041	1.542
$\Delta V_{OS}/\Delta T [\text{nV}/^{\circ}\text{C}]$		-20.43	18.31	-0.614	7.193

CMRR is also important in precision amplifiers and is defined by the offset variation across the common-mode range. Table 5 shows the PVT result obtained from Monte Carlo simulation with 100 runs. As been expected, the CMRR is also improved by 1,000 times, same as  $V_{OS}$ .

**Table 5.** Chopper operational amplifier - CMRR vs. temperature and process variation.

Param.	Temp. [ $^{\circ}\text{C}$ ]	$V_{DD}=0.9\text{ V}, V_{SS}=-0.9\text{ V}$			
		Min.	Max.	Mean ( $\mu$ )	Std. Dev ( $\sigma$ )
CMRR[dB]	-40	110.2	156.3	126.1	8.939
	25	111.3	156.7	124.8	8.923
	125	106.5	192	120.2	10.85
		$V_{DD}=1.65\text{ V}, V_{SS}=-1.65\text{ V}$			
	-40	116.8	162.5	132.5	10.47
	25	116.6	168.5	130.8	8.344
	125	118.2	166.4	130.6	10.05
		$V_{DD}=2.75\text{ V}, V_{SS}=-2.75\text{ V}$			
	-40	117.8	181.9	132.4	9.115
25	114.5	193	130.4	10.37	
125	113.8	163.7	126.8	9.49	

Fig. 22 and Fig. 23 shows the frequency characteristics of CMRR and PSRR. The chopper operational amplifier has a common mode rejection of at least 75 dB for frequencies below 100

Hz. The PSRR- has also a minimum of 75 dB for frequencies below 100 Hz while PSRR+ has a minimum of 130 dB.

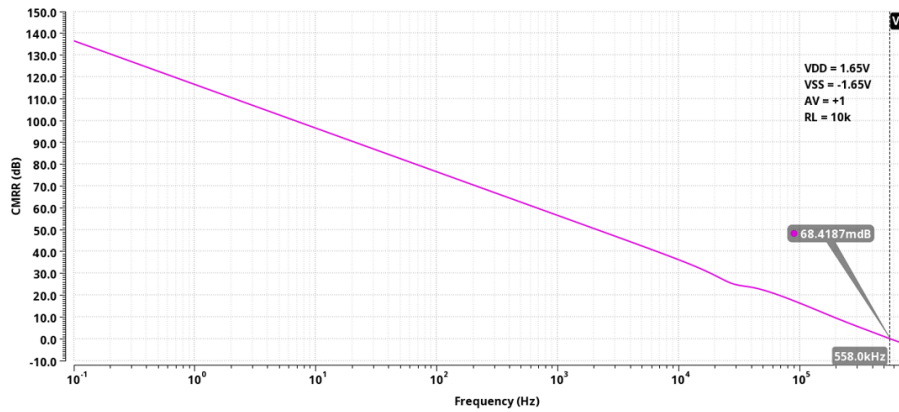


Fig. 22. Chopper operational amplifier – CMRR vs. frequency.

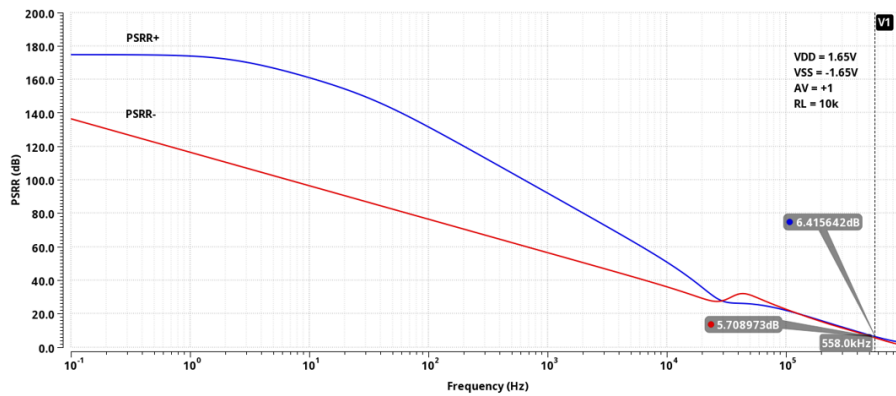


Fig. 23. Chopper operational amplifier – PSRR vs. frequency.

Table 6 shows the PVT results for PSRR, related to chopper offset-stabilized operational amplifier. The minimum simulated PSRR value is 121.2 dB.

Table 6. Chopper operational amplifier - PSRR vs. temperature and process variation

Param.	Temp. [°C]	Min.	Max.	Mean ( $\mu$ )	Std.Dev ( $\sigma$ )
PSRR [dB]	-40	125.2	187.8	140.2	10.66
	25	121.4	170.2	138.9	8.811
	125	121.2	192	137.6	11.28

Open Loop Voltage Gain of the chopper operational amplifier (Table 7) was also simulated for supply voltages of 1.8 V, 3.3 V and 5.5 V. A mean value of 124.3 dB and a minimum of 107.2 dB (at low temperature) were obtained.

**Table 7.** Chopper operational amplifier - Open Loop Voltage Gain vs. temperature and process variation

Param.	Temp. [°C]	$V_{DD}=0.9\text{ V}, V_{SS}=-0.9\text{ V}$				
		Min.	Max.	Mean ( $\mu$ )	Std. Dev ( $\sigma$ )	
AVOL [dB]	-40	110.9	174.6	127.4	10.29	
	25	111.7	179.6	138.1	10.48	
	125	118.4	171.9	138.7	10.08	
			$V_{DD}=1.65\text{ V}, V_{SS}=-1.65\text{ V}$			
	-40	108	153.9	126.3	9.735	
	25	121.7	184.2	142.2	9.759	
	125	127.1	182.7	138.3	9.813	
			$V_{DD}=2.75\text{ V}, V_{SS}=-2.75\text{ V}$			
	-40	107.2	169.9	124.3	10.29	
	25	120.8	177.4	136.3	10.45	
	125	129.2	160.3	139.6	8.94	

All the chopper offset-stabilized amplifier parameters presented above meet the precision operational amplifier requirements: low offset voltage, low noise, high CMRR, PSRR, AVOL etc.

Table 8 compares this work to other chopper operational amplifiers. It proves that the designed amplifier is competitive in terms of unity gain bandwidth (UGBW), offset voltage, even noise (considering supply current to noise ratio).

**Table 8.** Comparison with state-of-the-art

	<b>This Work</b>	<b>[3]</b>	<b>[10]</b>
Year	2020	2015	2006
Technology	0.25 $\mu\text{m}$	0.028 $\mu\text{m}$	0.6 $\mu\text{m}$
Supply voltage	1.8-5.5 V	0.9 V	1.8-5.5 V
Chopping frequency	100 kHz	500 kHz	125 kHz
DC Gain	107 dB	106 dB	106 dB
UGBW	558 kHz	329 kHz	350 kHz
Inputreferred offset standard deviation	0.85 $\mu\text{V}$	2.2 $\mu\text{V}$	–
Offsetvoltage (mean + standard deviation)	3.4 $\mu\text{V}$	–	3 $\mu\text{V}$
Input voltage noise density, en	50.13 nV/ $\sqrt{\text{Hz}}$	27 nV/ $\sqrt{\text{Hz}}$	55 nV/ $\sqrt{\text{Hz}}$
Supply current	36 $\mu\text{A}$	60 $\mu\text{A}$	17 $\mu\text{A}$

## 5. Conclusions

A new, efficient constant-gm technique was proposed, designed and simulated in a 0.25  $\mu\text{m}$  CMOS process. The circuit maintains a constant transconductance for rail-to-rail input stages operated in weak inversion. This is achieved with a much lower current consumption, eight times lower than in classical techniques. Moreover, the proposed constant-gm topology does not modify the output currents of the rail-to-rail input differential pairs.

With this technique, the total transconductance varies by at most 4% within the entire input common-mode voltage range (from  $V_{SS} - 100$  mV to  $V_{DD} + 100$  mV).

The proposed constant-gm technique was used in order to improve a chopper offset-stabilized operational amplifier performances. Low current consumption of the constant-gm circuit helped in achieving a quiescent current of the operational amplifier of only  $36 \mu\text{A}$ . In addition, the constant-gm architecture maintains unity-gain frequency almost constant for the whole range of common-mode voltage and supply voltage ( $1.8 \text{ V} \div 5.5 \text{ V}$ ).

The addition, the constant-gm technique led to a slight improvement of the main amplifier offset voltage and CMRR. These improvements, plus similar ones applied to the null amplifier, were implemented into the chopper offset-stabilized amplifier and led to very good simulated performances without a sizeable increase of current consumption: voltage noise density of  $51 \text{ nV}/\sqrt{\text{Hz}}$ , offset voltage of  $\pm 5 \mu\text{V}$ , minimum CMRR of 106 dB and GBW of 550 kHz for a quiescent current of  $36 \mu\text{A}$ .

As expected, chopper stabilization reduced the offset voltage of the main amplifier by three orders of magnitude and removed the  $1/f$  noise almost completely. The drawback is a worse transient response and settling time due to the additional signal path.

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