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Behavioral Modelling of Analog Computing Circuit for a Synapse of any Neuron in Artificial Neural Networks

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Abstract. Analog implementation and behavioral modelling of neural network computing for artificial intelligence AI is demonstrated in this work. The main advantages of this solution are the low count of semiconductor devices and low power consumption. The calculations are performed in real time and not with clock cycles, as compared to the digital approaches. A behavioral model of an analog multiplying circuit for a synapse of any neuron in artificial neural networks was developed in the paper to demonstrate the proof of concept and simulate its operation. The operation of the analog circuits resulted in very good concordance with the mathematical formula it is supposed to implement. The application of the behavioral model concerning the technological variation of parameters like the MOS transistors threshold voltage resulted in demonstrating a low margin of error. In conclusion, this circuit proves to be very suitable for neural networks in real-time, low power and low device count operations.

Key-words: Analog multiplying; artificial intelligence; behavioral model; neuron synapse; real-time and embedded systems; signal processing.

1. Introduction

Artificial intelligence has risen extensively in the present, using trained neural networks [1], [2], usually implemented in a digital system containing a great number of parallel processing units, that model the neurons of the network and their synapses (weights or ponders). The common operations done by the neurons are MAC-type (multiply and accumulate). Multiplication is completed between neuron outputs and the weights of the next neuron, and the results are added afterwards to form a new output. This multiplying operation is especially using many computing resources in the digital mode, implying besides calculation time substantial energy consumption. Also, analog circuits can be used for multiplication, e.g. the classic Gilbert cell [3]. The concept is quite old, being unveiled in 1968 [4]. In 1990, the same author designed a current-mode approach to his circuit [5].

In this paper, an analog circuit is studied for neural network operations, with the main advantages real-time processing and low energy consumption. The purpose is to minimize the calculation error of the bipolar and MOS multiplying analog circuits, using simulation models. This study was performed by varying specific model parameters and evaluating the results. The main advantage of simulation model's usage is shortening the simulation times, allowing to perform any kind of analysis, from simple one – transient to complicated – corner case simulations. The novelty of this study consists in this modeling part which provides the users with a new method for investigation: to configure the multiplying block, to simulate it in any use case and in the end, to be used as input to the neural networks - practically, the neuron will be the simulation model of the multiplying cell.

To perform MAC (multiply and accumulate) operations with an analog circuit some choices must be made. For example, voltage or current signals can be used. When voltage signals are chosen, after multiplication of the signals (neuron outputs and weights), the sum needs to be performed by an adding circuit usually implemented with an operational amplifier [6].

On the other hand, using current signals for operations, the adding can be simply made in a node, as given by the first law of Kirchoff. This solution eliminates the need for an operational amplifier for each neuron, therefore minimizing the number of components.

Also, the solution for the analog computing circuit can be implemented in bipolar or MOS (metal-oxide-semiconductor) technology. Since the exponential dependence of the current-voltage characteristics of the device is used to perform multiplication, the bipolar junction transistor (BJT) seems to be the device of choice. The BJT is a current controlled device, by the current injected in the base region. In this case, the base currents act as residual currents, ignored in the first approximation. Conversely, by choosing to implement the circuit with MOSFETs (MOS field-effect transistors) the problem of the base currents is eliminated because the MOSFET gate is isolated from the conducting channel and the device is voltage controlled on the gate terminal. In this case, to be able to use the exponential dependence of the current with the gate voltage, the sub-threshold conduction mode must be used [7]. This design approach proved viable and low power devices were designed recently based on this mode of operation [8]. They are also taking advantage of the latest technology GAA (gate-all-around) [9]. The advantage of this mode of operation is that the current values are lower than in the above threshold mode, ensuring lower energy consumption per device. For this study, both solutions (BJTs and MOSFETs) were analyzed, and conclusions will be presented. Behavioral modelling has the purpose of showing the overall operation of the circuits and to estimate the influence of variable device factors like the current gain and threshold voltage.

In the following, Section 2 describes the circuit mode of operation with a comparison of power consumption between bipolar and MOS versions and Section 3 contains the behavioral modelling of the circuits, with the obtained results following the variation of the main circuit and technological parameters. Section 4 concludes the paper.

2. The Multiplying Circuit

2.1. The Model of a Synapse

The synapse of an artificial neural network performs the multiplication of the input signal from the previous layer (the arrows pointing to the neurons of the hidden layer for example) with the weight (ponder) of the respective neuron. The mathematical model of the synapse is:

$$S_{out} = W_n S_{in}. \tag{1}$$

S_{in} is the signal received from the previous neuron, W_{n} is the weight of the neuron and S_{out} is the signal provided to the neuron. These three can be voltages or they can be also currents. There are hardware implementations where the weight is the conductance of a resistor. In this respect, the hardware model consists of a multiplying circuit, in this case in analog implementation, presented in Fig. 1. The input is the current IG1 and the weight is the current IS2. They are multiplied by the operation of the circuit given next with mathematical equations.

2.2. Bipolar Implementation

The circuit is presented on Fig. 1, using bipolar transistors [10]. In this circuit, the sum of V_{be1} and V_{be2} is equal to the sum $V_{be3} + V_{be4}$. This results in the multiplication of IG1 and IS2 currents, according to the following calculations:

$$\begin{gathered} V_{be1} + V_{be2} = V_{th} ln(I_{c1}/I_s) + V_{th} ln(I_{c2}/I_s) = V_{th} ln(I_{c1} I_{c2}/I_s^2) = \\ V_{be3} + V_{be4} = V_{th} ln(I_{c3} I_{c4}/I_s^2). \end{gathered} \tag{2}$$

The result is:

$$I_{c2} = I_{c3} I_{c4}/I_{c1} = I_{G1} I_{S2}/I_{S1}. \tag{3}$$

Here $V_{th} = kT/q$ is the thermal voltage, with k the Boltzmann constant, q the elementary electric charge and T the absolute temperature. The emitter currents were approximated with the collector ones (base currents neglected). The transistors are considered identical, having the same saturation current I_s.

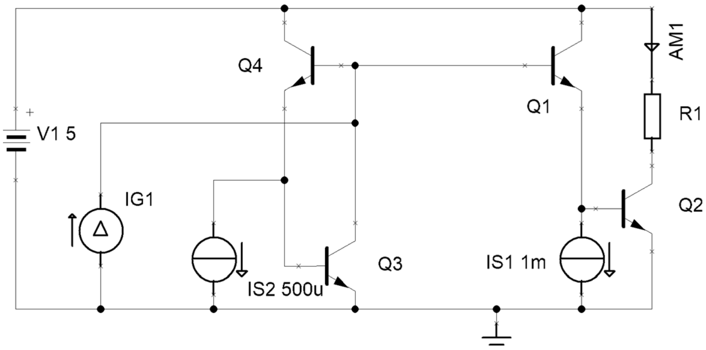

Fig. 1. Example of a multiplication circuit in bipolar implementation [10].

The same result is obtained using MOS transistors operating in sub-threshold regime, where the relation between the drain current and the gate-to-source voltage is exponential, like in the case of the bipolar transistor.

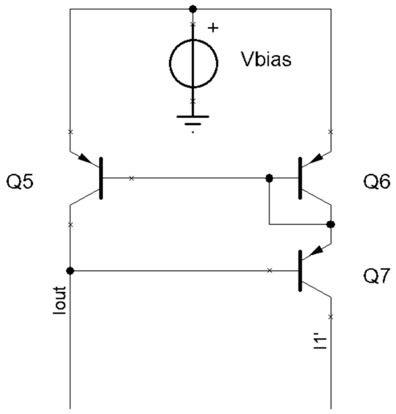

Fig. 2. Output stage to transform the current for the next layer [11].

In Fig. 1, Q3 has $V_{ce} = 2V_{be}$, so the circuit can be supplied with a voltage as low as 3 volts. Since $I_{out} = I_{c2}$ is a sinking current, to drive the next network layer (current IG1) the circuit in Fig. 2 is used to transform it into an outbound current. $I_{c7} = I_{c6} + I_b = I_{c5} + I_b = I_{out}$. The transistors are supposed to be identical. The bias current IS1 for the circuit in Fig. 1 (and for current IS2 as ponder) is provided by the circuit in Fig. 3, a classic Widlar current source [11].

Because $V_{ce8} + R_2 I_{bias} = V_{be2}$ in Fig. 1, it is suitable I_{bias} be smaller than the output current I_{out} (and IS2 smaller than IG1) so Q8 is not in saturation regime. Simulations show that IG1 and I_{out} can be in the range 10. . . 100 µA while IS2 and I_{bias} in range of 1. . . 10 µA. With MOSFETs in the sub-threshold regime the currents can have lower values.

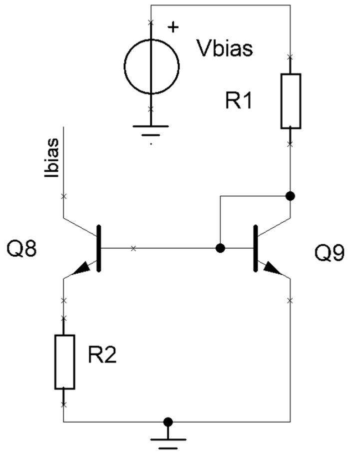

Fig. 3. Current mirror for Ibias, Widlar current source [11].

Since the operation of the multiplier circuit is based on the exponential dependence of the current with the voltage, the current range must fall in the exponential region of the characteristics as in Fig. 4. Note the semi-logarithmic scale. Therefore, the operating collector currents of the circuit must be in the 100pA to 10mA range. Also, to ensure good value for the current gain of the bipolar transistors, the collector current should be above 10nA.

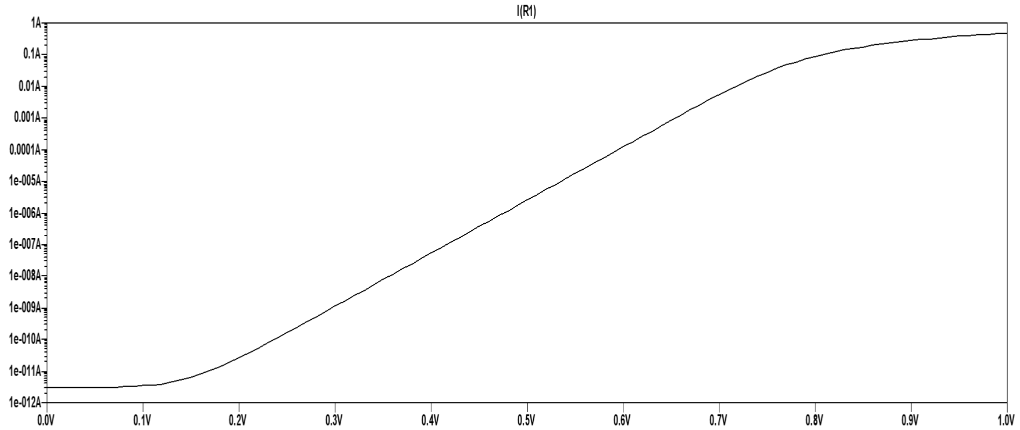

Fig. 4. Collector current dependence on the base-emitter voltage for a 2N2222 bipolar transistor.

For a MOS transistor, the exponential dependence of the current is obtained in the subthreshold region, as shown in Fig. 5. Also in this figure, the current is shown at logarithmic scale.

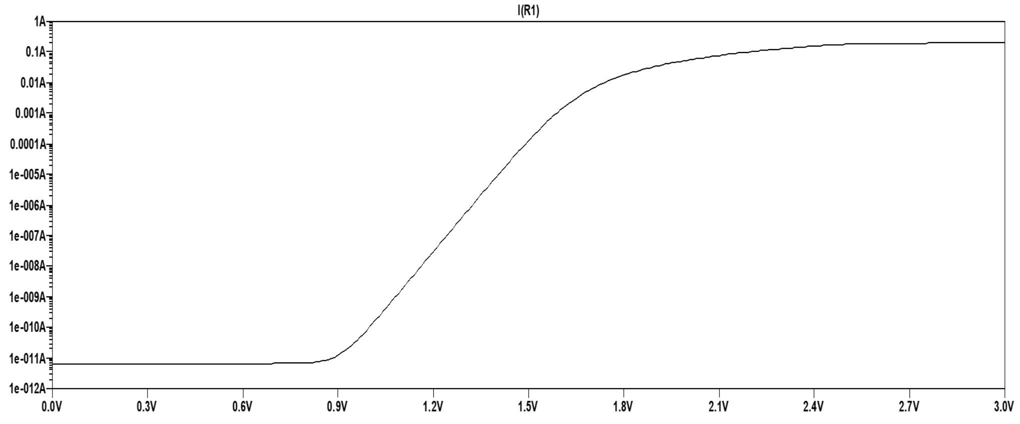

Fig. 5. Drain current dependence on the gate voltage for a BSP89 MOS transistor. In this case, the useful current range is 100 pA to 1mA.

2.3. MOS Implementation

The implementation of the complete synapse circuit is shown in Fig. 6: multiplication, base current and output current conversion. The multiplication is done with M1 to M4 nMOS transistors, M7 and M8 implement the reference current and M5, M6 implement the transformation of the output current from sink to outbound, if necessary. Note that unlike the case of the current mirror with bipolar transistors in Fig. 2, there is no need for a third transistor, since MOSFETs have no input current into the gate, while BJTs need base current, so Q7 is needed for the compensation of the base currents into the output current.

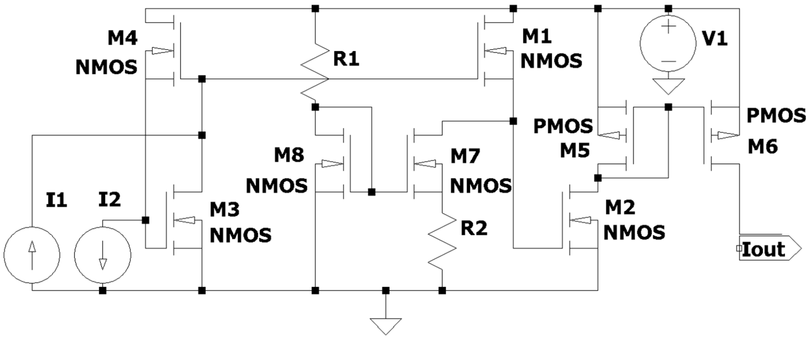

Fig. 6. The multiplication circuit realized with M1 – M4 nMOS transistors, the reference source M7 and M8 and the output current conversion with M5, M6 pMOS transistors.

It is interesting to compare the power consumption of MOS circuit and bipolar circuit. As noted, for bipolar version the range of the currents considered being 1nA to 1mA so with a voltage supply ($V1$ or $Vbias$) of 3 to 5 volts and 5 branches of current results the range 15 to 25 nW to a maximum 15. . . 25 mW. For the MOS variant of the circuit, with currents in the range 100pA to 100nA and a voltage supply of 3 volts the maximum power consumption is at 1.5 µW.

The power levels in the case of MOS variants are much lower, as shown in Table 1, so it is recommended as a circuit of choice for integrated circuit implementation.

Table 1. Power consumption of the multiplying circuit

Simulation models	Bipolar version	MOS version
Current value/Supply voltage	5V	3V
100pA		1.5nW
1nA	25nW	
100nA		1.5 µW
1mA	25mW	

The results concerning the power consumption levels are a continuation of another work of same authors [12] dealing only with MOS technology. The next development of this work is the behavioral modelling in the next Section, that allows not only the analysis of the multiplication circuit, but also the inclusion in a larger system, namely a neural network, as shown below.

3. Results

3.1. Behavioral modelling

In recent years, the focus of the electronic industry has been to reduce the entire development time of the ICs, but at the same time achieve best-in-class results, and ultimately, make a quantum leap forward. In this regard, a new approach has been developed, behavioral modeling [13], [14]. So, a user/customer can easily test functionality without using the hardware part.

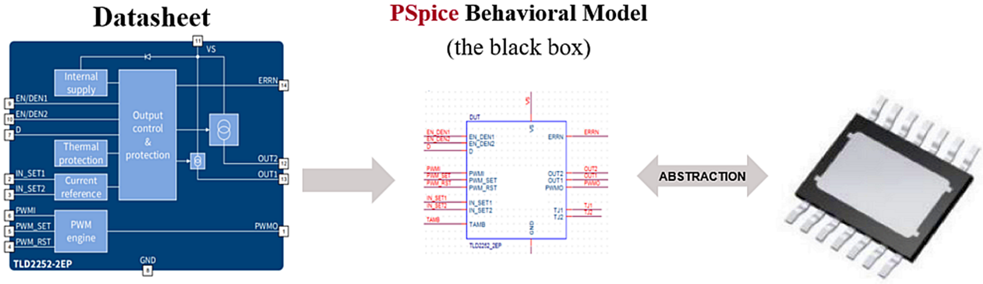

Fig. 7. Definition of behavioral modeling [15].

Also, the system simulations are on focus, using behavioral models from different ICs to achieve the entire circuit application. DC-DC converters, gate drivers, smart power switches are just some examples of the ICs which can have associated a behavioral model, but in the end, any IC can have a behavioral model because it is an abstraction of the reality, giving the product's datasheet, like shown in Fig. 7.

Practically, a simulation model is a software representation of an IC which covers all specifications and required functionalities.

In this article, the multiplication circuit and the current reference circuits presented in Figs. 1-3 and 6 are implemented as parametrical behavioral models based on PSpice simulator. This is an advantage in modeling, because, once the model is developed and validated, it can be reused in any analog simulator like: OrCAD, LTspice, Tina, SIMetrix etc. Another advantage is that nothing is destroyed or burned, any test case can be implemented and investigated without negative consequences in a very short time. This is the main reason why customers or users prefer to use simulation models in these unpredictable times, being considerably cheaper than a demo board which reflects the functionalities of the IC in a certain use case. Of course, there are some challenges when a simulation model is developed: convergence issues and the possibility to obtain an idealized behavior.

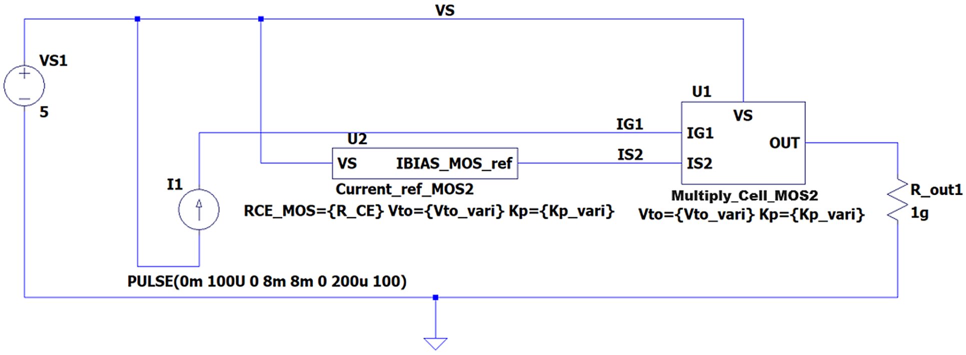

Fig. 8. Test bench: Simulation model the current reference and multiplying cell.

The modelling steps are the creation of schematics as in Fig. 8, then running Monte Carlo analysis with the variation of relevant parameters for bipolar and MOS technologies.

Table 2. Model configuration

Component	Name	Value/model
Supply voltage	Vs	5V
Current reference	IS1 (internal current)	Bipolar: 2µA; MOS:20µA
Ratio current	IS2	Bipolar: 500nA; MOS: 40µA
Current from the previous neuron	IG1	Bipolar: 20µA; MOS:100µA
Bipolar transistor	-	2N2222
nMOS transistor	-	BSP89

3.1.1. Multiplying behavioral models

This article proposes two multiplication behavioral models – one based on the bipolar models (2N2222) and the other one based on the nMOS models (BSP89). Practically the main analog circuit is simplified and the active components from Fig. 1 are modeled. Moreover, the current reference circuits are modeled which provide the IS1/ IS2 currents to be able to study the output current response closer to the reality.

The study was done in time domain using Monte Carlo variations in 200 points for each case. The test circuit is presented in Fig. 8 and the components used for model development are listed below, in Table 2. The simulation models prove the mathematical assumptions shown in the beginning of this study, so, the simulation results, the output current (marked in blue) and the current formula, determined in equation (3), are simulated as shown in Figs. 9 and 10.

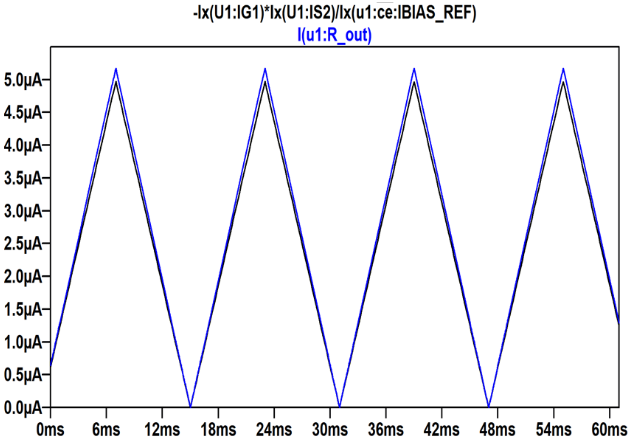

Fig. 9. Bipolar results.

It can be noticed that for the bipolar implementation, the output current is a little bit bigger (with 100nA) than the expected results (mathematical formula), and this comes from the transistor current gain (β factor) – if β is bigger, the results will be closer. On the second implementation, based on the nMOS transistors, the results are the same, but 1.5uA is the difference just on the current peaks. This is caused by the K_p – transconductance parameter. If its value is increased, the current peaks overlap perfectly.

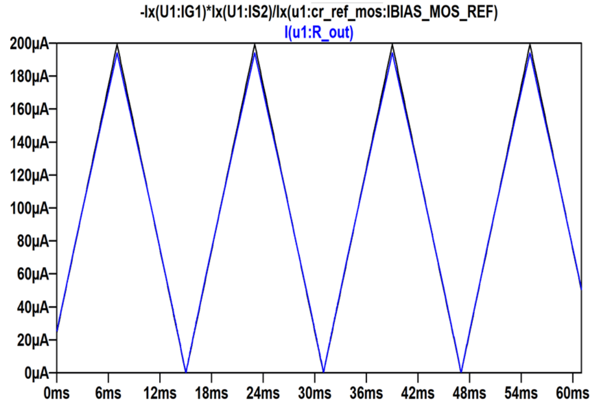

Fig. 10. nMOS results.

In another work [12], it is shown that the error of multiplication is less than 0.1% at a specified temperature (and due to technological process variations) which is similar to the one of Gilbert cell [16], but the Gilbert Cell has three inconvenient features: (1) its X input is a differential current; (2) its output is a differential current; and (3) its Y input is a unipolar current [16], (1) and (2) making it not suitable for artificial neural networks application. In this way, the simulation models are validated, and the analog computation is done, using the active components, running in sub-threshold regime. Moreover, the experiment fulfilled the expectation, the nMOS implementation is more performant than the one based on the bipolar transistors in terms of accuracy of the output current overlapping over the mathematical calculus and total simulation speed.

3.1.2. Monte Carlo analysis

Monte Carlo analysis [17], [18] analyzes the effects of the errors trying to prevent possible damage during operation due to different electronic circuit parts. It is performed simultaneously with different types of analysis like transient, AC analysis, DC sweep and so on.

Thus, this paper performs this kind of analysis considering the tolerance of 10% and the interested parameters are presented below (Table 3).

Table 3. Monte Carlo parameters of interest

	Parameter	Definition	Default value
nMOS	V_{th}	Threshold voltage	1.6V
model	K_p	Transconductance	1.1 µA/V^2
Bipolar	I_S	Saturation current	1fA
model	β	Current gain	75

The total number of runs was 200 (each bipolar and nMOS), and the resulting Gaussian distribution demonstrates the robustness of the simulation models. Normal distributions or Gaussian distributions are the key to interest in statistics [19], [20]. They are commonly used in science to represent real-valued random variables whose distributions are not known.

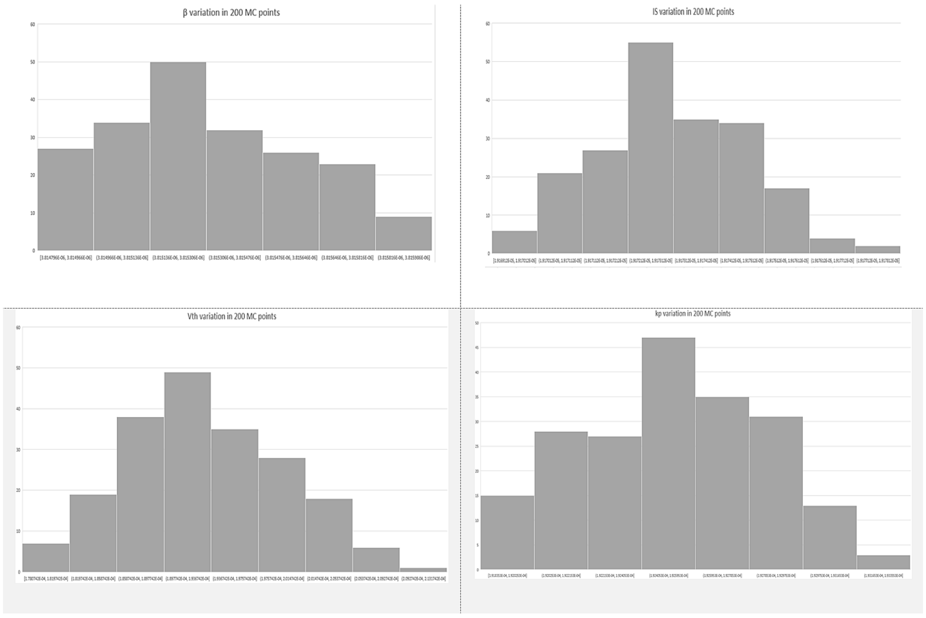

Fig. 11. Gaussian distribution for different model parameters.

The central limit theorem explains that, under certain conditions, the mean and variance of the average of many samples of a random variable are themselves random variables. As the number of samples increases, distribution of the random variable converges toward a normal distribution. Because of this, physical quantities expected to be the result of many independent processes (e.g., measurement errors) often have near normal distribution.

The results are presented in the graphs of Fig. 11, proving the robustness of the multiplying circuit, the values are centered to a one point – mean value and it can also be observed the standard deviation which determines the width of each graph.

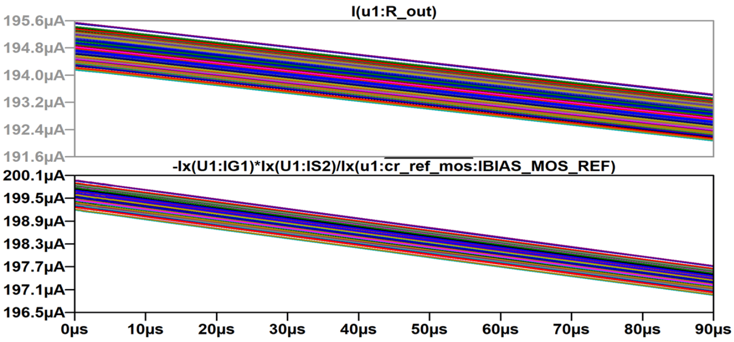

Fig. 12. K_p parameter variation in Monte Carlo analysis – comparison between the output current and mathematical calculation.

Moreover, Fig. 12 presents a graphs comparison between the current output of the multiplying circuit and the math calculus, which are very close to each other. In this figure, it can be observed that the relative error regarding the current output is maximum 0.72% for all variations of K_p parameter. As mentioned before, the error gets lower with an increased value of K_p.

Thus, the study demonstrates the usability of the simulation models, and the results indicate the correctness of them in comparison with the mathematical formulas which represent a state of the art and the starting point of this paper.

4. Conclusions

In this work a behavioral model of an analog multiplying circuit was developed to simulate its operation. The results demonstrate the correct operation of the circuit in comparison with the mathematical formula of multiplication. Also, the behavioral model and Monte Carlo analysis demonstrated technological feasibility. Such circuits have low power consumption, low component count and real-time operation in comparison with digital circuits. By comparing the bipolar version of the circuit with the MOS version with respect to power consumption, the obvious choice is MOS technology.

The main contributions are obtaining power consumption results and behavioral modelling with Monte Carlo analysis, which shows the possibility of the expansion of this circuit at whole neural network scale with minimal errors.

As a next step, neural experiment based on the bipolar and nMOS multiplying simulation model is planned to be developed in the future in MATLAB/Simulink.

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