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Implementation of Semi-Static and Differential Null Convention Logic Gates Using CNTFET Technology

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Abstract. This paper aims to implement NULL Convention Logic gates using CNTFET technology. NCL is a clockless technique to solve timing problems, and CNTFET is a low-power technology in comparison to the others. Hence high performance and efficient circuits with low power and low delay can be obtained by combining the two techniques. In terms of power, latency, power delay product, and transistor count, various asynchronous *NULL Convention Logic* (NCL) gates semi static, and differential have been implemented using CNTFET technology and is compared with the existing CNTFET based NCL static gates, based on the observations gates suitable for adder design is identified. Differential NCL gates have low power and better PDP when compared to both static and semi-static NCL gates. The number of transistors used for differential NCL logic gates are minimum equivalent to semi-static logic and are lesser than static NCL gates. All the simulations are carried out using CNTFET 32nm technology in cadence virtuoso tool and the results obtained prove that the CNTFET based differential logic gates are efficient enough in terms of delay, power consumption and PDP.

Key-words: NCL Logic, logic gates, CNTFET, low power, low delay.

1. Introduction

New developments in the manufacture of CMOS integrated circuits allow for incredibly small feature sizes on chips, resulting in ICs that are substantially smaller and have a lot faster clock rate. Even though the clock rate speeds up synchronous logic architectures, it could increase power consumption and result in many clocks concerns with distribution. Despite dominating the semiconductor industry for decades, synchronous design today limits the system's performance to the worst-case delay, especially for systems with clock speeds nearing GHz.

The asynchronous architecture, on the other hand, can handle issues such as clock skew, jitter, power consumption, and noise so on and it concentrates on local handshaking for synchronization, providing a ready to use SoC, as well as increased toughness for process variations as well as performance in data-dependent and event-driven environment delayed systems. Asynchronous circuits can be conceived and implemented in a variety of methods, *Null Convention Logic* (NCL) [1] is one of the most promising method. As indicated in Table 1 [2], NCL circuits are made up of 27 state-holding threshold gates [3], which make up the set of all four-variable functions. Each gate is represented by THmnWw1w2w3 [4], with m signifying the gate threshold, n the number of inputs, and w1, w2, and w3 the input weights.

Table 1. Fundamental NCL gates [2]

NCL Gate	Boolean Function
TH12	A+B
TH22	AB
TH13	A+B+C
TH23	AB+AC+BC
TH33	ABC
TH23w2	A+BC
TH33w2	AB+AC
TH14	A+B+C+D
TH24	AB+AC+AD+BC+BD+CD
TH34	ABC+ABD+ACD+BCD
TH44	ABCD
TH24w2	A+BC+BD+CD
TH34w2	AB+AC+AD+BCD
TH44w2	ABC+ABD+ACD
TH34w3	A+BCD
TH44w3	AB+AC+AD
TH24w22	A+B+CD
TH34w22	AB+AC+AD+BC+BD
TH44w22	AB+ACD+BCD
TH54w22	ABC+ABD
TH34w32	A+BC+BD
TH54w32	AB+ACD
TH44w322	AB+AC+AD+BC
TH54w322	AB+AC+BCD
THxor0	AB+CD
THand0	AB+BC+AD
TH24comp	AC+BC+AD+BD

For example, when at least two of the three inputs of a TH23 gate are asserted, its output gets asserted. As hysteresis is present with NCL gates, once asserted, the outcome will remain maintained till the inputs are all de-asserted. When m equals n, the NCL gate is the same as a C-element [5] with n inputs. Dynamic, static, semi-static [6], and differential [7] NCL gates have all been implemented in CMOS. The dynamic mode of NCL gates is not considered because it is not delay-insensitive. The implementations of C-elements that are static and semi-static have been extensively addressed in [8]. The paper [9] recently introduced and explored the NCL implementation in differential mode.

CNTFETs [10, 11] are high-density [13, 14], high-performance [15], and low-power circuits, [16]. The CNTFET technology offers a solution to the CMOS technology's scalability [12] restrictions. Threshold voltage of the transistor can be changed by changing the diameter of CNT (DCNT) or the chirality vector [17, 18], which refers to atoms arranged in an angular pattern along the tube (Vth). Circuits implemented using CNTFET technology avail the advantages of low power consumption, high electron mobility, low threshold voltage, reduced gate leakage current and not direct tunneling. Hence this paper aims to utilize the advantages of CNTFET technology to enhance the performance of NCL logic circuits.

The various NCL gate CMOS implementations [19–21] and CNTFET based NCL static logic are explained in Section II, and the new CNTFET based semi-static and differential gates are introduced and implemented in Section III. Section IV presents simulation results for several NCL gates realizations, and Section V draws inferences from comparisons.

2. Existing Work

A. Static NCL gates

For the set and reset functions, synchronous gates normally have one network of pull-ups and pull-downs, which are complementary. However, delay-insensitivity is provided to the NCL gates through hysteresis, with pull-up and pull-down network added additionally to maintain the resultant value when neither the set nor the reset functions are true, as the set and reset functions in NCL gates are not complementary. The auxiliary networks are known as Hold1 and Hold0. The block diagram of static mode NCL is shown in Fig. 1. The transistor count in Static NCL logic can be lowered by sharing each pair of pull-up or pull-down network transistors. It is also worth noting that Hold0=$\overline{\text{Set}}$ and Hold1=$\overline{\text{Reset}}$.

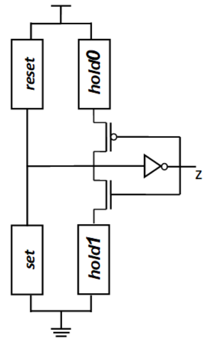

Fig. 1. Structure of Static NCL gates [1].

B. Semi-Static NCL gates

In semi-static mode of realization, a weak feedback inverter replaces the Hold1 and Hold0 networks, as demonstrated in Fig. 2. Regardless of whether the set or reset functions are used, the charge on the Y internal node of Fig. 2 is maintained. Size of the weak inverter should be cautiously chosen. The inverter in the feedback should be weak so that the pull-up network will not be able to deliver sufficient assertion current to overcome it and reset the output. A weak inverter in the feedback, on the other hand, will not be able to compensate for internal node charge loss or sink/source enough current to tolerate noise on the Y in the case of pull-down network charge sharing. Charge sharing can be avoided if the transistors in the pull-down network are carefully placed [19], but the weak inverter must be able to tolerate noise on the internal node and restore charge if charge sharing occurs. The NMOS channel width is usually reduced to make the feedback inverter weaker, but if the inverter is not weak enough even with the smallest width, the NMOS channel length is increased.

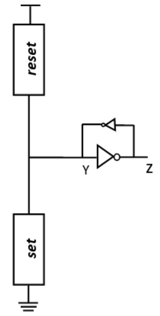

Fig. 2. Structure of semi-static NCL gates [2].

C. Differential NCL gates

The differential mode of realization of NCL gates [8] is very analogous to a *Differential Cascode Voltage-Switch Logic* (DCVSL) [20–23] except that inverters in cross-coupled mode are used as an alternative to PMOS cross-coupled transistors [9–12]. An NCL gate in differential mode is exhibited in Fig. 3.

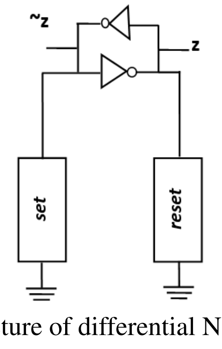

Fig. 3. Structure of differential NCL gates [2].

The main change among the semi-static and differential implementations of NCL gates is that the reset block now uses a pull-down network to connect output Z to ground. The reset block must now use NMOS transistors rather than PMOS transistors owing to this change in circuit architecture, necessitating the usefulness of input complements. Because each differential NCL gate provides both output Z and its complement, no additional circuitry is required to invert inputs. Asserting one output in a differential NCL gate demands pulling the other low via a pull-down network (either set or reset block); as a result, both outputs are always low for a brief while before they flip value. There is never any conflict between pull-down blocks in a design built with NCL differential gates since the differential gate inputs come from the other differential gates outputs. The differential implementation is improved in a variety of ways due to implementation of NMOS transistors in the reset block which have high mobility compared to PMOS. This is because the reset block is now stronger than before, making it easier to alter the state of the cross-coupled inverters. As a result, the differential method is usually faster than the semi-static method. Furthermore, because the differential implementation requires less scaling, it is frequently smaller than the semi-static technique. A differential NCL gate be able to generally work with the minimum sized transistors. Furthermore, owing to the evenness of the differential realization, the cross-coupled inverters are generally scaled evenly, making the entire structure less susceptible to size and hence more robust to PVT variations.

All the efficiencies of these designs can be further enhanced by implementing them with CNTFET technology files.

Literature usually treats CNTFET-based NCL static logic gates but because the review shows that semi-static and differential NCL gates are better in terms of speed and size. This study focuses on constructing semi-static and differential NCL gates utilizing CNTFET technology to add the low power benefit to the existing benefits.

3. Designing of Semi-Static and Differential NCL gates using CNTFET Technology

As previously stated, the benefits of NCL can be amplified when utilized with CNTFET technology. CNTFET has already been used to build static NCL logic. As a result, the focus of this paper is on designing all 27 NCL gates as shown in Table 1 in semi-static and differential mode utilizing CNTFET technology.

NCL Semi-static gates implementation using CNTFET technology:

For TH12 semi-static NCL gate with A, B inputs and Z output, Z is given by:

$$Z = A + B, \tag{1}$$

and its circuit diagram is shown in Fig. 4.

Fig. 5 shows the THxor0 semi-static NCL gate with A, B inputs and Z output, Z is given by:

$$Z = A^{*}B + C^{*}D. \tag{2}$$

NCL Differential gates implementation using CNTFET technology:

Fig. 6 shows the TH12 Differential NCL gate with A, B inputs and Z output, Z is given by the following equation:

$$Z = A + B. \tag{3}$$

Fig. 7 shows the THxor0 Differential NCL gate with A, B inputs and Z output, Z is given by the following equation:

$$Z = A^{*}B + C^{*}D. \tag{4}$$

All the other NCL gates are also implemented in semi-static and differential modes, and their outputs are recorded.

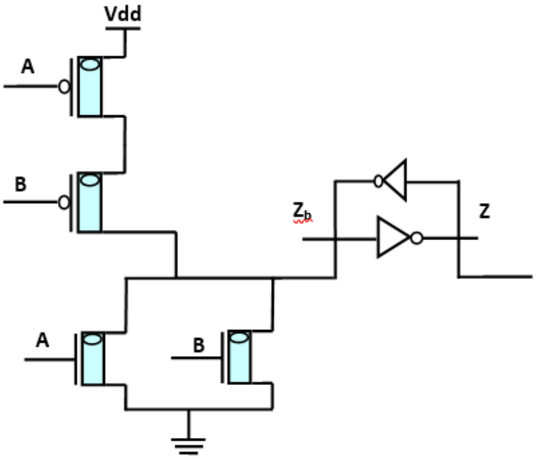

Fig. 4. CNTFET based TH12 Semi-Static NCL gate.

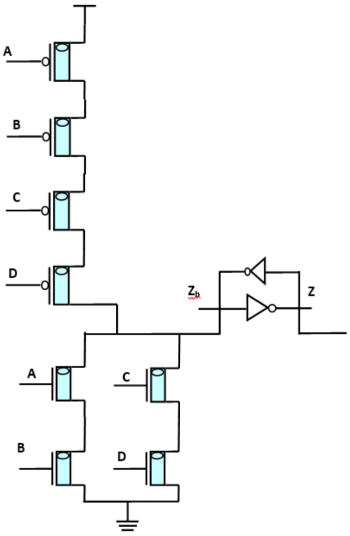

Fig. 5. CNTFET based TH12 Semi-Static NCL gate.

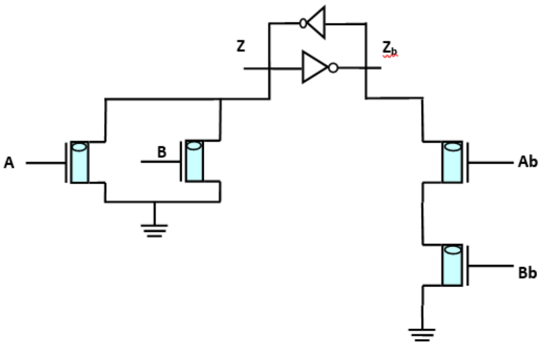

Fig. 6. CNTFET based TH12 Semi-Static NCL gate.

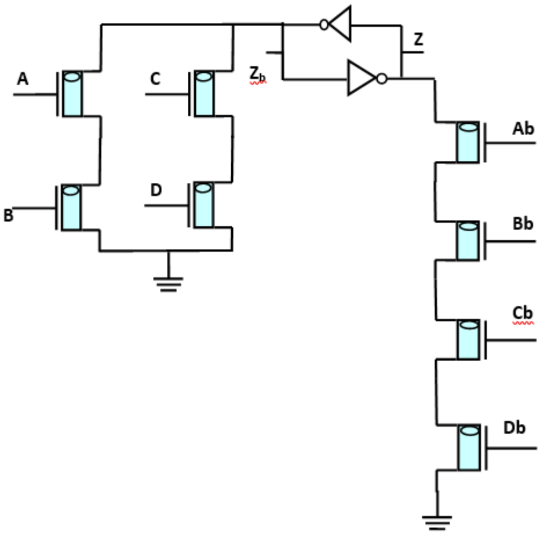

Fig. 7. CNTFET based TH12 Semi-Static NCL gate.

4. Simulation Results and Comparison

In static, semi-static, and differential modes, all 27 NCL gates are simulated to have a fair comparison. The findings show that differential mode gates have an excellent power-delay product, making them appropriate for application in computational circuits. As a result, differential mode gates can be employed to create half and full adder circuits that confirm the prediction. Figs 8-34 show the simulation results of the semi-static and differential mode NCL gates implemented in cadence with virtuoso platform with a supply voltage of 0.9 V. All these figures are saved in webpage [24]. All the results prove that the designs are efficient enough in providing full swing output.

From the results represented in Table 2 it can be proved that the differential design is efficient in terms of delay and power, due to its logic implementation using higher-mobility NMOS transistors instead of PMOS transistors in the reset block and because of less scaling required, as it is usually smaller than the semi-static approach requiring less power. Power Delay Product (PDP) of all the 27 gates simulated in static, semi-static and differential mode is shown in the graph mentioned in Figure 35. These results prove the efficiency of differential mode implementation of NCL gates to obtain complementary outputs which are required to drive the other stages with the same transistor count as that of the semi-static. The transistor counts comparison report of all the NCL gates in the three different styles mentioning the N-transistor and P-transistor count separately is shown in Table 3.

Table 2. Comparison report of NCL gates

S.No	NCL GATES	DELAY (p Sec)			POWER (p W)		
		STATIC	SEMI-STATIC	DIFFERENTIAL	STATIC	SEMI-STATIC	DIFFERENTIAL
1	TH12	5	45	10	228.3	163	154.5
2	TH22	4	25	22	813	243.3	123
3	TH13	7	50	22	165.6	135.1	144.2
4	TH33	12	56	30	173.1	150.6	136.7
5	TH23W2	10	44	20	298.2	167.8	98.47
6	TH33W2	5	38.5	32.5	274.3	170.6	154.6
7	TH14	7.5	35	10	644.4	185.4	95.01
8	TH24	10	45	20	970	199.6	156.2
9	TH34	10	47	17	3703	1250	161.9
10	TH44	7.5	34	12.3	1390	530.5	402.1
11	TH24W2	6.5	35	16	1405	172.1	140
12	TH34W2	10	45	17	1614	162.5	153.6
13	TH44W2	8.5	40	20	1375	180.2	164.2
14	TH34W3	10	35	15.9	1726	156.1	139.2
15	TH44W3	20	45	25.5	1270	160.2	145.6
16	TH24W22	42	35	29.1	1232	172.2	139.5
17	TH34W22	10	45	16.2	1458	171.8	154.8
18	TH44W22	12.5	44.5	21.2	1921	1727	634.1
19	TH54W22	20	27.5	16.2	1381	150.4	142
20	TH34W32	20	35	15.3	182.4	138.2	1248
21	TH54W32	15.2	45	26.2	1372	199.7	144.8
22	TH44W322	15	45	26.4	1431	166.4	152.5
23	TH54W322	20	45	26.9	1585	153	139.5
24	THxor0	22.5	45	25.9	1392	162	145.8
25	THand0	20	45	26.5	1424	304.3	152.5
26	TH24comp	20	35	25	1406	353.8	118.6
27	TH23	10	24	16	257.8	140.2	137.5

5. Conclusions

This paper focuses on designing a low power and low delay logic circuits. It achieves speed by using NCL semi-static and differential logic and low power by using CNTFET technology files. Hence these gates are very efficient in terms of speed and power compared to the existing designs and are also efficient in comparison to CNTFET based NCL static logic too. All the

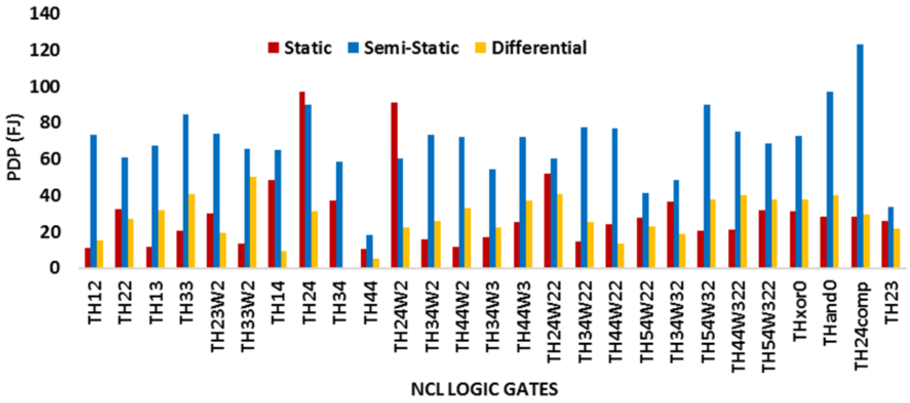

Fig. 8. PDP of NCL gates.

Table 3. Comparison report of NCL gates

S.No	NCL GATES	Transistors (PCNT+NCNT)		
		STATIC	SEMI-STATIC	DIFFERENTIAL
1	TH12	6+6	4+4	2+6
2	TH22	6+6	4+4	2+6
3	TH13	8+8	5+5	2+8
4	TH33	8+8	5+5	2+8
5	TH23W2	8+8	5+5	2+8
6	TH33W2	8+8	5+5	2+8
7	TH14	10+10	6+6	2+10
8	TH24	15+15	6+11	2+15
9	TH34	15+15	6+11	2+15
10	TH44	10+10	6+6	2+10
11	TH24W2	12+12	6+8	2+12
12	TH34W2	13+13	6+9	2+13
13	TH44W2	13+13	6+9	2+13
14	TH34W3	10+10	6+6	2+10
15	TH44W3	10+10	6+6	2+10
16	TH24W22	10+10	6+6	2+10
17	TH34W22	13+13	6+9	2+13
18	TH44W22	12+12	6+8	2+12
19	TH54W22	10+10	6+6	2+10
20	TH34W32	10+10	6+6	2+10
21	TH54W32	10+10	6+6	2+10
22	TH44W322	12+12	6+8	2+12
23	TH54W322	12+12	6+8	2+12
24	THxor0	10+10	6+6	2+10
25	THand0	11+11	6+7	2+11
26	TH24comp	12+12	6+6	2+10
27	TH23	10+10	5+7	2+10

three NCL logic styles static, semi-static and differential, are simulated and compared in terms of power, speed, power delay product, and transistor count. Based on the results, it has been concluded that differential mode of implementation achieves even more speed as it uses only NMOS transistors for logic implementation and has low power consumption due to less scaling required, as it is usually smaller than the semi-static approach requiring less power. Hence energy efficient adder designs could be implemented using these CNTFET differential mode NCL gates as they produce complementary output with same transistor count.

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