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Battery Connected Linear Voltage Regulator for Very Low Current Consumption Automotive Applications

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Abstract. This paper presents a battery connected linear voltage regulator suitable for always-on automotive applications (keyless entry, car monitoring, anti-theft system). The regulator is designed as a simple 3 pins device and it is always connected to the battery, even when the car's engine is off; therefore, a very low quiescent current of the regulator is mandatory. The regulator has a fixed 5 V output voltage and can deliver up to 0.5 A to the load. The total quiescent current of the proposed regulator is 3.8 μA at no load and due to an adaptive biasing technique a value of 75 μA is achieved at 500 mA load current. The architecture include a buffer to bias the gate of pMOS pass device and so a PSRR value of 65 dB at 100 Hz is obtained. Moreover, being supplied directly from the automotive battery, this regulator can withstand the very harsh environment in terms of temperature, line disturbances, EMC. The proposed regulator was implemented on silicon in a 0.8 μm BiCMOS technology and its characteristics were simulated and measured.

Key-words: pMOS; power supply rejection ratio; very low quiescent current.

1. Introduction

The automobile is considered as one of the greatest inventions of the 20th century. With the increasing development of electronic technology, electronic devices embedded in automobile has shown significant advantages in aspects of controllability, comfortability and safety. Currently, electronic components comprise 30-40% of total costs for almost all automotive categories and due to this, in this paper we will focus on power management in automotive vehicle [1]. With more and more electronic modules installed on cars, the increasing power demand and load versatility complicate the power management system.

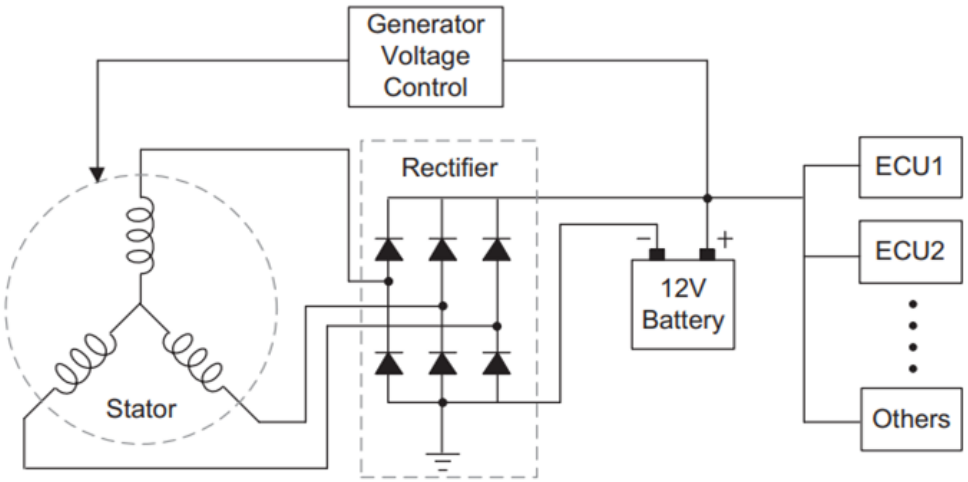

Fig. 1. A simplified automotive power management system [1].

Fig. 1 shows a simplified power management system in a car. This system handles the battery charging through a generator (stator and rectifier). The generator voltage control regulates the generator output voltage to 12V. The battery is supplying power to separate *electronic control units* (ECUs) and other electric modules. Modern cars can feature an average of 100 ECUs, such as airbag control unit, body control module, engine control unit, brake control module and so on [2].

Normally, many electronic devices inside the ECU need lower voltage for operating than this battery voltage which unfortunately it is not too stable (depends on loading or other external conditions that could be very difficult to predict). Therefore, a power management module with DC voltage conversion and power supply rejection is essential.

The power supply solution in the ECU (Fig. 2) is usually a voltage regulator and depending on the application, it is implemented as a linear or a switching mode power supply or a combination of the first two solutions.

This paper is an extended version of [3] and presents a linear voltage regulator suitable for always-on automotive applications (keyless entry, car monitoring, anti-theft system). It means the regulator is always connected to the battery, even when the car's engine is off and, therefore, a very low quiescent current of the regulator is mandatory. Since the output voltage is linearly regulated, aspects like dynamic response, output noise and power supply rejection are optimized. From the power efficiency perspective, this regulator does not optimize it too much, but it compensates with reliability and really low cost compared to other supply solutions.

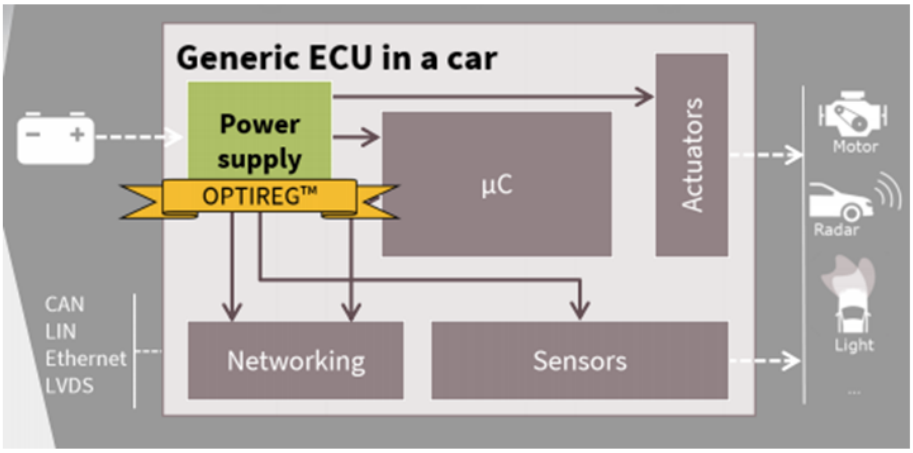

Fig. 2. Automotive ECU [2].

2. Specifications

In this paper, the focus is to design a linear voltage regulator which is directly connected to automotive battery; so the input voltage (V_I) has 13.5V typical value, but according to the automotive standards it can vary in a wide domain (7 to 40V) corresponding to different conditions (cold cranking, slow discharging, load dump, load jump etc.).

The regulator needs to supply the microcontroller in the ECU with a fixed 5V output voltage (V_o) and it needs to deliver 500mA maximum output current. The dropout voltage should not exceed 400mV @ 100mA output current and 2V @ 500mA output current (including process variation and temperature variation from -40 °C to 150 °C).

The output voltage of the regulator should remain in $\pm$ 2% in steady state and $\pm$ 10% when full range load steps occurs. Additionally, the regulator should have a minimum 60dB PSRR at 100Hz and the output voltage should not exceed 5.5V (values above considered dangerous for the application) when fast large signals are applied on the input ($\Delta V_I/\Delta t = 100$ V/ms).

The most challenging requirement is the quiescent current. It should be smaller than 4μA when the regulator has no load at the output and smaller than 100 μA when a 500mA current is drawn from the regulator.

The device should be implemented in a 0.8μm BiCMOS technology that includes two kind of devices: low voltage devices (7V class) and high voltage device (45V class). To reduce the chip area (by using low voltage devices), a pre-regulator is required. It needs to generate a voltage lower than 7V which will supply the internal blocks of the linear regulator.

3. Proposed Architecture

Proper design of a linear voltage regulator involves intrinsic knowledge of the system and its load. The tasks of minimizing the quiescent current, optimizing load/line regulation and PSRR performance, maintaining stability and minimizing transient output voltage variations prove to be challenging and often conflicting. This arises from the specific characteristics of the regulator architecture and its associated working environment.

The dropout specification forces us to choose an architecture with pMOS as the pass element and this means a proper stability performance of the regulator should be achieved.

The proposed architecture is depicted in Fig. 3. It includes: a pre-regulator, a Bandgap voltage reference, a pMOS pass device, an error amplifier with a resistive feedback network. Error amplifier consists in an operational transconductance amplifier (OTA) followed by a buffer which controls the pass transistor gate. Based on Fig. 3, the output voltage VO can be expressed as:

$$V_O = (1 + R_1/R_2) \cdot V_{REF} \tag{1}$$

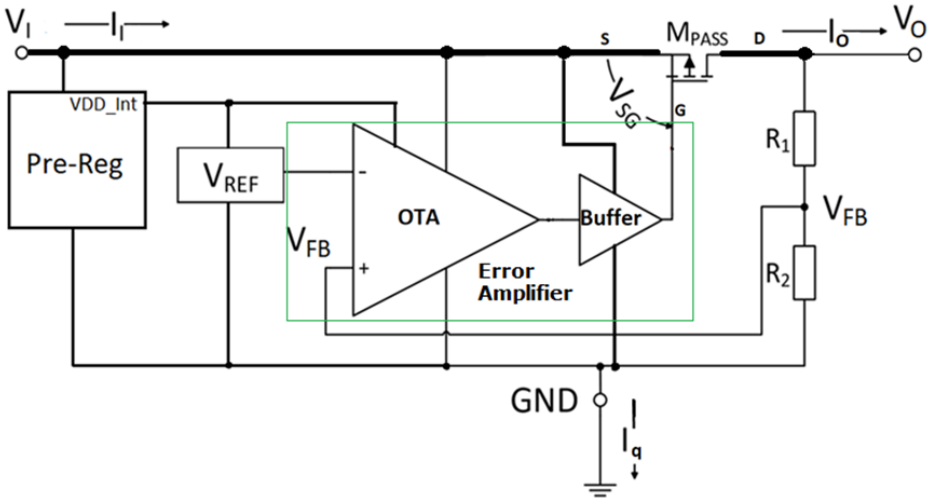

Fig. 3. Block diagram of the proposed system [3].

The pre-regulator generates an internal voltage rail of about 4V and supplies the voltage reference and the OTA. It is implemented by a Zener voltage reference ($V_Z = 5.6$V) which is buffered by an nMOS common drain stage. The block has an approximate 0.5μA quiescent current and offers two main advantages: 1) allows the usage of low voltage devices in reference voltage block and in the OTA; 2) protect the internal circuitry by filtering the harsh disturbances on the battery supply rail.

The ideal voltage reference should be a voltage insensitive to changes in temperature, supply voltage and process variations. It is obvious that every variation of V_{REF} translates into an output voltage variation, in this case amplified (1). Because of quiescent current constraints and due to its robustness, a Brokaw Bandgap voltage reference [4] was implemented. V_{REF} block generates a first order temperature compensated voltage of about 1.2V and it has a total quiescent current of about 0.5μA. For reducing the total quiescent current of the regulator, a 200nA bias current needed for the OTA is also generated in the voltage reference block without adding too much extra circuitry.

The input voltage domain impose the voltage class of the pMOS pass device and both dropout voltage and maximum power dissipation specifications gives the size of the transistor. Therefore, the pass device is a 45V class pMOS transistor with an aspect ratio of 40000 (at minimum length of the technology for this kind of device).

Named "error amplifier (EA)", this block amplifies the voltage difference between the reference and the feedback voltage and generates an error signal that controls the pass element in order to regulate the output voltage. Both *operational transconductance amplifiers* (OTA) and *operational amplifiers* (op-amp) could be solutions for error amplifier implementation in linear regulators. Since an OTA has a high output resistance, its output resistance and pass device transistor gate capacitance can be combined together to form a dominate low frequency pole, which is referred to as internal compensated regulator. This is a good solution for some capacitor-free linear regulator structures. For these structures, the low output capacitance leads to a high frequency output pole (outside the desired bandwidth), so the system can be designed as a single pole system [2].

A common way to drive the gate of the power transistor in order to obtain an externally compensated linear regulator (the output pole is the dominate one) is by using an op-amp (cascading an OTA and a buffer – Fig. 3) [5]. Since the gate pole is situated at higher frequencies due to lower output resistance of the op-amp, the output pole becomes the dominate one (for output capacitors in microfarad range), but any other internal poles will add difficulties for frequency compensation. The proposed regulator uses a similar technique and this will be detailed in the following part.

4. Proposed Regulation Loop

The regulation loop includes the error amplifier (OTA + buffer), the pass device and the resistive divider (Fig. 4).

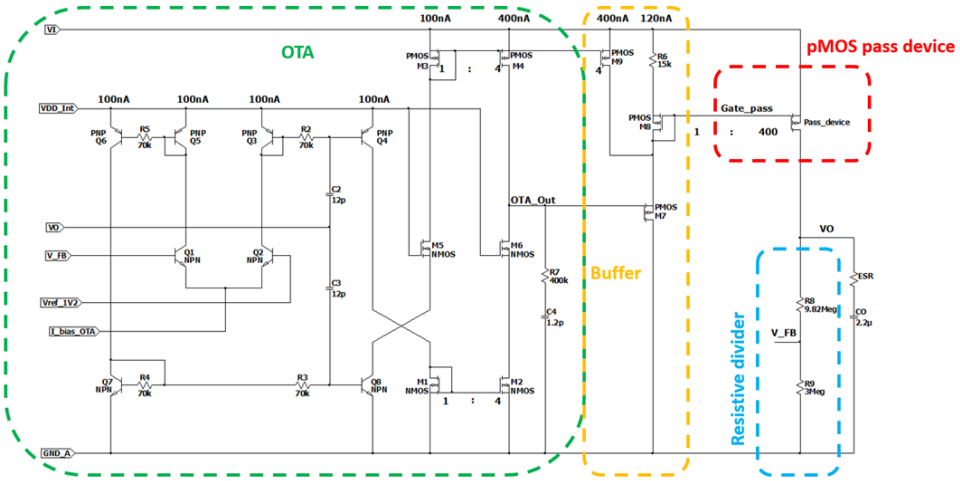

Fig. 4. Proposed regulation loop [3].

The error amplifier characteristics are directly related to the static and dynamic performance of the linear regulator and therefore, the design of error amplifier is the key for regulator design. Transient performance, PSRR and especially the stability are quite challenging to achieve when having a pMOS architecture and a very low budget of current consumption.

The proposed OTA in the regulation loop (Fig. 4) is a symmetrical one and composed from

two parts:

- a low voltage part supplied from the pre-regulator via VDD_Int pin and implemented with low voltage bipolar transistors: $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7, Q_8$
- a high voltage part supplied directly from the input voltage rail: $M_1, M_2, M_3, M_4, M_5, M_6$.

The high voltage part translates the signal from the low voltage domain to the high voltage domain in order to control the buffer (supplied from the input voltage). For increasing the slew-rate in OTA_Out node, M_1, M_2 and M_3, M_4 current mirrors have a multiplicity of four. The differential pair uses a 200nA bias current that is generated in voltage reference block. Considering this low level of currents flowing through the amplifier's branches, a proper sizing (low aspect ratio and low area) of the MOS transistors was done to avoid the subthreshold operation and to minimize the effect of leakage currents.

The buffer is implemented with a pMOS transistor configured as source follower and offers a relative low output resistance of the error amplifier (approximately 1/gm7). Therefore, the pole associated to the pass device gate moves to higher frequencies (small signal) and for large signal, the slew-rate in the gate of pass device increases considerably. Moreover, considering that the output pole frequency is changing as the load current changes, an adaptive bias current with the load current is used for the buffer. M_8 is a fraction of pass device and due to its connections, it injects a fraction of output current into pMOS buffer (supposing R_6 is zero, M_8 and pass device work as a current mirror with an ratio of 400) – meaning the output resistance of the error amplifier is changing with the respect of output current. From stability perspective, this solution make our life easier because now, when output current changes, the gate pole is moving together with output pole. R_6 acts as a degeneration for $M_8 - M_{pass}$ current mirror and its effect is to limit the current through the pMOS buffer at high output currents; at low output currents, the voltage drop on it is low (few mV) and its effect is negligible. Also at very low output currents (0 to few hundreds of μA): M_8 mirrors the load current, but due to relative high mirroring ratio (400), the bias current for the buffer becomes very small (2.5nA at 1μA load). For this reason, M_9 is used to add a 400nA bias current into the pMOS buffer by copying the output stage current of the OTA.

Already mentioned, the stability of the loop is critical and for this reason the low frequency poles in the loop were identified (Fig. 4.):

- the output pole(V_O) pole : p_1 – given by the external output capacitance and output resistance of the pMOS pass device
- the gate pole (Gate_pass): p_2 – given by the parasitic capacitance of pMOS pass device and the output resistance of the buffer
- the output of the OTA pole (OTA_Out): p_3 – given by the parasitic capacitance at the input of the buffer and the output resistance of the OTA
- the feedback node pole (V_FB): p_4 – situated at relative high frequencies compared to the firs three poles and it is given by the parasitic capacitance of the differential input pair and the equivalent resistance of the resistive divider.

Therefore, at least two low frequency zeros are needed in the transfer function in order to ensure the stability.

The proposed OTA implementation allows the usage of two symmetrical R-C pairs (R_2, C_2 and R_3, C_3) which will help for assuring the stability by introducing a zero in the transfer function and cancel the effect of the first of the three poles. This compensation technique [6] use a capacitance multiplier effect with Q_4 and Q_6. For large signal, the two pairs highly improve the transient response by creating a fast path from the output to the gate of pass device and reduce considerable the undershoot and overshoot at the output. The second zero is introduced with an additional R-C pair (R_7, C_4). It cancel the effect of the pole in OTA_Out node. The output capacitor (C_O) and its series resistance (ESR) introduces an extra zero in transfer function.

Summarizing, they are three low frequency poles and two low frequency zeros in the loop. The zeros frequencies were chosen in order to make the circuit stable over the process, temperature, input voltage and output current domain.

From the quiescent current point of view, the regulation loop has three main contributors: OTA, buffer and resistive divider. OTA consumes 900nA approximately; the buffer consumes 520nA at 50μA load and about 70 μA at 500mA load; and the resistive divider, having a total resistance of 12.82MΩ (3MΩ +9.82MΩ) consumes about 400nA. The regulation loop has an overall quiescent current of 1.8μA at 50μA load (this value for output current value represents the minimum expected current that can be consumed by the application – in our case the microcontroller in an ECU).

5. Results

The proposed regulator is implemented in a 0.8μm BiCMOS silicon technology and its characteristics were simulated and measured.

Fig. 5 shows the simulated DC characteristic of the regulator for four output currents (25°C). Dropout voltage was measured as the difference between input and output voltage when the output voltage is 4.9V (regulator goes out of precision). For I_O=100mA dropout voltage is 201mV and for IO=500mA, a value of 943mV is obtained. These values are in line with the initial specifications. The regulator has 7V as minimum input voltage, but Fig. 5 shows that already at 6V the regulator enters in the regulation region at 6V for all output currents (T=27°C, nominal corner).

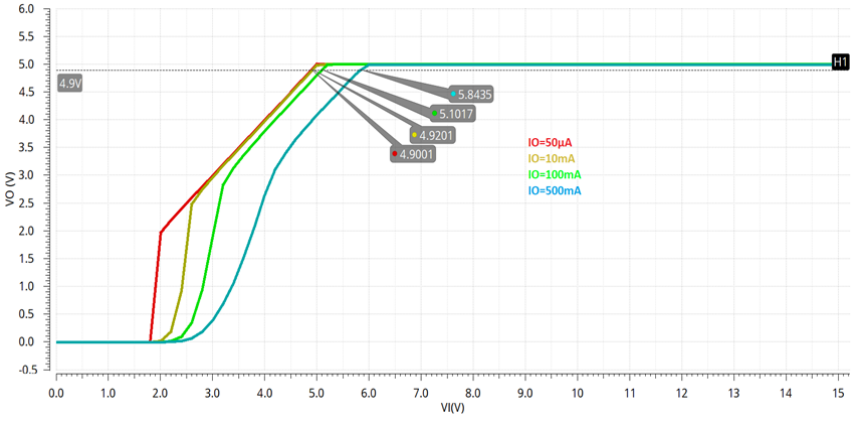

Fig. 5. V_O versus V_I (4 output currents) [3].

The output voltage was measured at different temperatures and for four different output currents. Fig. 6 show the temperature variation of the output voltage which replicate very accurate the curvature of the Bandgap voltage reference (first order temperature compensated reference). From Fig. 6 we can extract the temperature coefficient (TC) of the regulator (about 20ppm/°C) and the load regulation in function of temperature with a maximum value of 0.03mV/mA at 150°C.

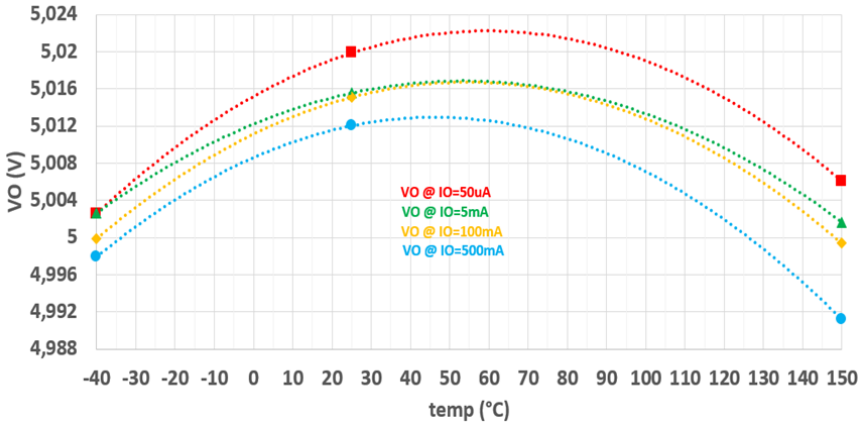

Fig. 6. V_O versus temperature (4 output currents).

The quiescent current I_q was measured for different load currents and at three temperatures and the measurement result is plotted in Fig. 7. Measurement was done for a single sample and with nominal input voltage (13.5V). At 25°C and 50μA load current, the total quiescent current of the regulator is 3.82μA, value which is smaller than the initial specification (4μA). At maximum output current (500mA), due to adaptive biasing of the buffer, I_q becomes 75.1μA, again smaller than 100μA which was the initial specification. An important observation is that the quiescent current increases with temperature as expected (bias current is generated as voltage reference over a negative temperature coefficient resistor – resulting in a PTAT current).

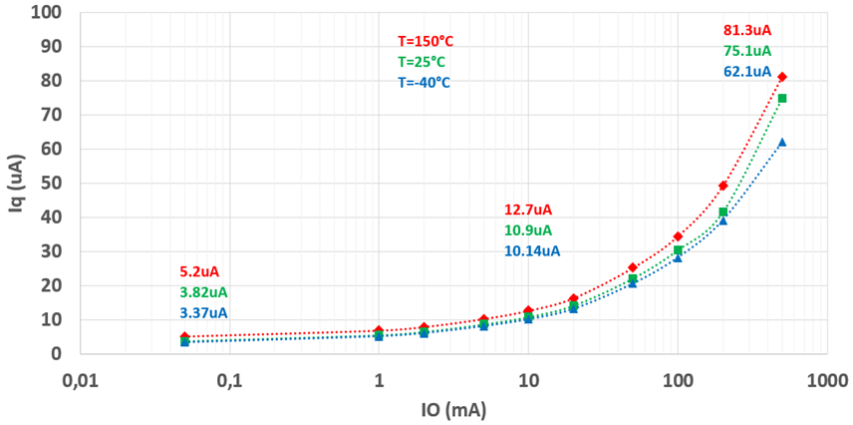

Fig. 7. Quiescent current versus output current (3 temperatures) [3].

In Table 1 the PSRR performance is illustrated. Both simulation and measurement confirms that regulator has about 65dB at 100Hz, with very small variations over the load current domain. At 1 kHz, PSRR values are still higher than 45 dB for medium to high output current range.

Table 1. PSRR [3]

I_O[mA]	Frequency			
	100Hz		1kHz	
	Sim.	Meas.	Sim.	Meas.
0.05	66.5	64.5	38	34
10	66.7	65.5	46.8	45
500	66.7	–	46.9	–

Fig. 8 shows the output voltage of the regulator when a positive load step (50μA to 500mA in 1μs) and a negative load jump are applied at the output (three temperatures). Using a 2.2μF output capacitor and a 13.5V input voltage, the measurement shows a maximum undershoot of 440mV at 150°C for positive load step, and a maximum overshoot of 340 mV for negative step also at 150°C.

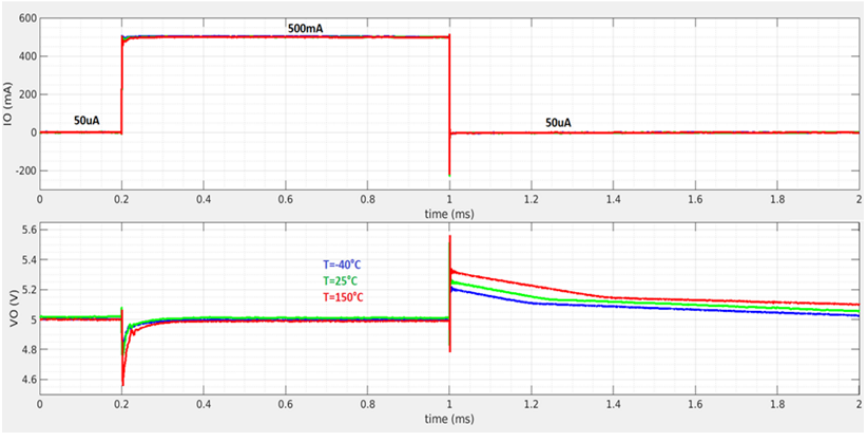

Fig. 8. Load transient response: (top) output current, (bottom) output voltage [3].

An important test for a battery connected automotive regulator is to apply a series of voltage spikes with high slew-rates (∼100V/ms) on the input and observe the behavior at the output. During this kind of tests, the output voltage should not exceed a maximum value depending on the application, in this case 5.5V. In Fig. 9 is shown the regulators response when jumps from 7V to 20V in 100μs are applied at the input. The measurement was done twice: for minimum output current (50μA) and for maximum output current (500mA). Even with this harsh perturbation, the attenuation is higher than 30 and the output voltage remains below 5.15V.

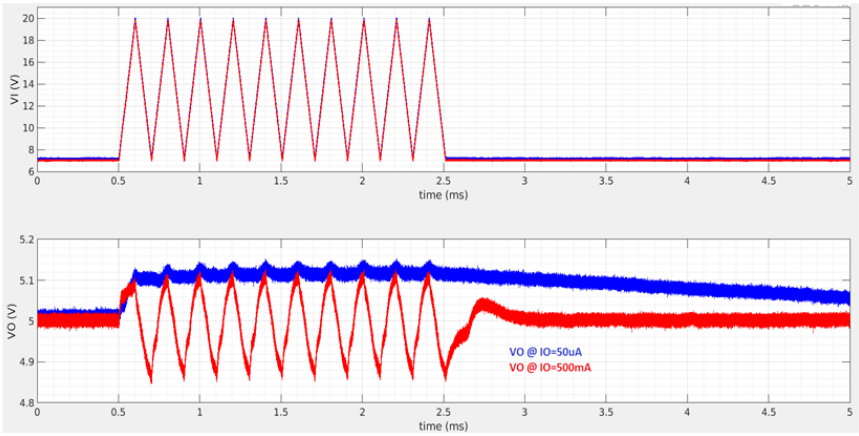

Fig. 9. Line transient response: (top) input voltage, (bottom) output voltage [2].

Table 2 illustrates a brief summary of the regulator's characteristics in comparison with [7] and [8]. Even with more challenging requirements in terms of input voltage domain and output current range, the performance of the regulator is comparable with the two for similar architecture and close current consumption. The proposed regulator shows similar PSRR performance compared to [7] and [8]. From static performance point of view (line and load regulation), this regulator is superior to the references. From transient perspective, it seems both references shows better performance. This is somehow justified by bigger load steps and bigger pass device (bigger parasitic capacitance) in order to accommodate a large output current.

Table 2. Performance summary [3]

Parameter	**I_O (mA)**	**[7]**	**[8]**	**Sim.**	**Meas.**
V_O(V)	–	1.2	2.8	5	5
V_I(V)	–	1.4–1.8	2.9–3.3	7–40	7–40
$I_{O,max}$ (mA)	–	50	150	500	500
I_q(μA)	0.05	1	5.2	3.62	3.82
	50	83	–	23.7	24
	500	–	–	74.7	75.1
PSRR(dB) (100Hz)	10	–	68	66	65
PSRR(dB) (1kHz)	10	46	52	46.8	45
C_O(μF)	–	0.47	1	2.2	2.2
R_{ON}(Ω)	–	4	0.67	2.01	1.92
Line reg. (mV/V)	500	7.25	6.75	0.037	0.120
Load reg. (mV/mA)	–	0.140	0.250	0.022	0.030
Max. under-shoot	–	18mV (0–50mA)	40mV (0–150mA)	435mV (0– 500mA)	440mV (0- 500mA)
Max. Over-shoot	–	7mV (50mA–0)	75mV (150mA–0)	325mV (500mA–0)	340mV (500mA–0)

6. Conclusions

This paper presents a very low quiescent current linear voltage regulator for automotive applications. The proposed regulator was implemented in a 0.8μm BiCMOS technology and its characteristics were simulated and measured. The device has a total quiescent current of 3.8μA at no load and due to the adaptive biasing of buffer, a 75μA was obtained at 500mA load current. Using the buffer, a PSRR of 65dB at 100Hz was obtained even with this very low quiescent current available. Load transient response shows a maximum 440mV undershoot and 340mV overshoot for full load step. Both simulation and measurement results confirms that all initial requirements were met.

Acknowledgments. This work is an extended version of [3] and it was realized in collaboration with Infineon Technologies Romania.

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