

Improved Serial Peripheral Interface Controller Based on Scan Architecture

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Abstract. A high performance, digital serial controller having a self-test-based architecture is presented. A standard architecture able to achieve the targeted functionality was modified in order to contain the test mode circuitry for testability improvements. After the importance of creating digital architectures adapted for testability is underlined, we present the high frequency serial controller for analog switches. This block was adjusted for test reasons and implemented into a 3 V CMOS technology. The block is integrated together with input-output pad structures forming an entire chip structure for which the layout was implemented. Based on schematic design simulations, timing checks and defects analysis, the proposed architecture is confirmed.

Key-words: Coverage; design for testability; digital controller; scan insertion; test mode.

1. Introduction

Nowadays life is mostly based and surrounded by means of technology, which are electronic systems manipulating data. These systems are in charge of storing, processing, and communicating information. Digital data manipulation is the concept that had a tremendous impact on the evolution of electronic systems. More and more applications which are being deployed in order to serve a broad range of domains are requiring complex digital architectures. The main metrics for quantifying the quality of a digital circuit are cost, functionality, robustness, performance, and energy consumption [1].

Serial Peripheral Interface (SPI), along with *Inter-Integrated Circuit (I2C)*, *Universal Synchronous Bus (USB)*, *Double Data Rate (DDR)* are just few examples of protocols highly employed in plenty of applications in different domains: automotive, automatization, consumer electronics, communications systems, etc.

The SPI protocol presumes the communication between a master device (e.g., a microcontroller - MCU) and one or many slave devices (sensors, converters, registers, memories). The microcontroller selects the slave device by driving low the Chip Select line connected to the intended slave circuit to communicate with it. Data is being transmitted from master to the slave through *Master Output Slave Input Line* (MOSI) or from slave to the master through *Master Input Slave Output* (MISO). The SPI transactions are synchronized by the Serial Clock signal emitted by the master device [2].

SPI multi-channel switches [3–7] can be found in applications like data acquisition, communication systems, input-output control, multimedia signal routing. These circuits distinguish through the capability of controlling the activation and deactivation of a certain number of analog switches not through a usual multiplexer [8], but by means of digital synchronous interface being controlled by a master device. Every switch activation/deactivation is driven by the values of one internal register written or read through SPI commands. Our recent CAS paper [7] presents a digital control block, where the standard serial architecture was improved for reaching very high clock frequencies up to 55 MHz, while working with voltages between 2.5 V ÷ 5.5 V, and within a temperature range between $-40\text{ }^{\circ}\text{C}$ ÷ $125\text{ }^{\circ}\text{C}$. That circuit was designed in 0.18 μm CMOS technology.

This paper is meant to bring adjustments to the standard design [7], targeting a better testability of the circuit itself. The block presented in [7] was re-designed, by inserting test mode circuitry, while maintaining the required functionality in user mode. The scan version of the serial controller proposed in [7], was designed in a 65 nm CMOS technology, able to operate with voltages up to 3.3 V, among a temperature range of $-40\text{ }^{\circ}\text{C}$ ÷ $125\text{ }^{\circ}\text{C}$. The same frequency upper limit was targeted, 55 MHz. From the functionality requirements, the user mode instructions: the read and write in one of the five registers are preserved and software reset command is maintained as well. For test mode, the digital block can detect test entry special commands and operate according to the imposed test methodology.

Besides this introduction, the paper is structured in five sections as follows: Section 2 offers background information on the Design for Testability topic, Section 3 describes the design and implementation of the initial serial controller, Section 4 presents the Scan SPI Controller's architecture. Section 5 shows the layout and defects analysis and simulations results. Finally, Section 6 concludes this article and reveals envisioned further steps.

2. Design for Testability – Background

A testable circuit is a circuit whose architecture is containing necessary circuitry to allow simple, efficient testing by means of access to inputs and outputs, all critical nodes have test points, power and ground rails are easy to check, the chains are able to check if data transmitted at inputs can propagate correctly throughout entire internal circuitry [9–12].

Internal Scan involves internal modifications to a logic design for increasing its testability. A general digital circuit contains combinational logic and sequential logic (e.g., data flip-flops). It may have a number of inputs (IN1, IN2, IN3, etc) and a number of outputs (OUT1, OUT2). After scan insertion, it gets two additional inputs (SC_IN and SC_EN standing for Scan Input Signal and Scan Enable Signal) and one additional output (SC_OUT standing for Scan Output Signal) (Fig. 1). Scan methodology supposes replacing all memory elements of a design with their scannable counterparts and then connecting them into scan chains structures [11].

Primary inputs are those inputs that can be controlled directly by the test environment. Primary outputs are the outputs that can be observed directly by tester.

Test patterns or test vectors are sets of 1's and 0's placed on primary input pins during manufacturing test processes to determine if the chip works as expected. These tests are performed with *Automatic Test Equipment* (ATE). When tests are applied, the ATE compares the output values of the chip with the expected values [12].

Scan cells which form scan chains are serving to ensure observability and controllability for the memory structures in the design (latches and flip-flops) [12]:

- controllability: ability to set certain logic values at each node in the circuit by driving the inputs of the circuit [10].
- observability: ability to derive the logic values of every node by controlling inputs and observing the values of the outputs [10].

The continuous research being developed for increasing testability of mixed signal circuits [13–16] indicates the suitability of further research on this topic.

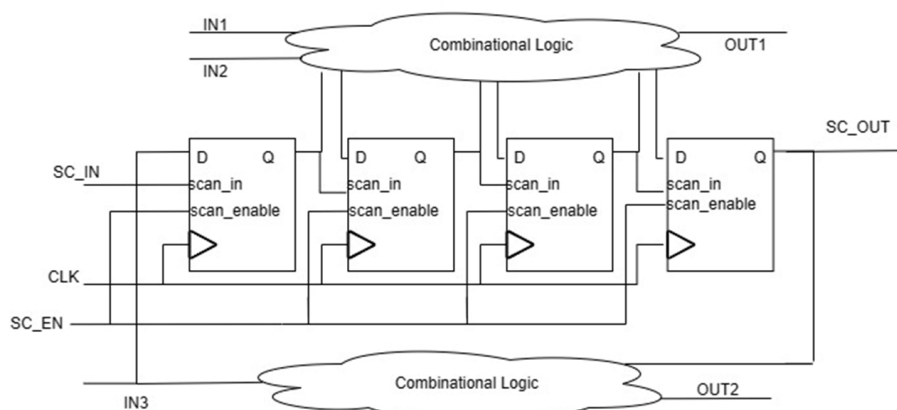


Fig. 1. Digital circuit after scan insertion.

3. High Frequency SPI Controller – Standard Implementation

A first implementation of the serial controller [7] was designed in a 180 nm CMOS technology, being able to operate with frequencies up to 55 MHz, for supply voltages between 2.5 – 5.5 V and within a temperature range of 40 °C ÷ 125 °C. Verifications were run on schematic and layout of this circuit for validating it.

Figure 2 illustrates a diagram of the block. The inputs of the circuit are: SCK - Serial Clock, CSB - Chip Select Bar, SI - Serial Input, RESETB - asynchronous Reset, PORB - Power-on-Reset. The outputs are: SO – serial output and Q [7:0] – eight parallel outputs meant to activate/deactivate switches [7].

The building parts of the proposed block (Fig. 2) are finite state machine meant to decode the instructions and provide internal signals for updating the registers bank, circuitry for providing and storing the default output code for serial output, bits counter, four storage registers (register at address 0×01 is controlling the switches) and a reset register. This serial block is Mode 0 SPI compliant [7].

As with every SPI transaction, for this block, the CSB line must be driven low by the master for starting a valid transaction (Fig. 2). Any command transmitted while PORB input is low will be rejected. This pin indicates if the supply voltage reached a steady state value or not. Together with RESETB, they serve as asynchronous reset inputs for the interface. The information communicated by the master to our block on the SI line is sampled on the rising edge of the clock. The output data, transmitted towards the master on the falling edge of the clock.

All logic transitions of the data input are being synchronized with the SCK clock signal and all outputs are expected to reach their final steady state values in one clock period after the changes in the inputs. This required the fact that the delay of the combinational circuitry to be much lower than the clock period, along with implementing a robust clock tree structure for driving the internal clock signals to the intended flip-flops.

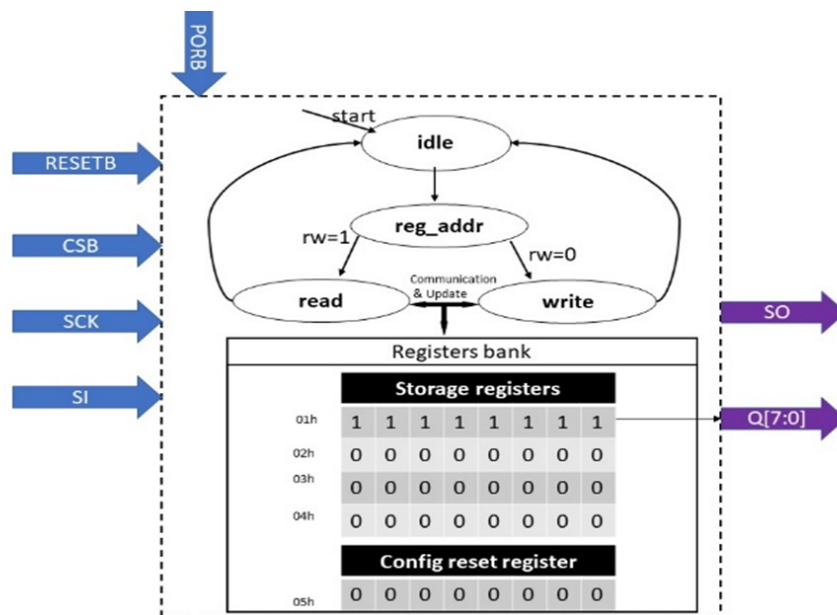


Fig. 2. Concept diagram for proposed SPI block [7].

Figure 3 depicts the layout of the digital block. Routing is done on metals M1–M3, metal M4 being left for wider supply and ground buses at top level.

The circuit was validated by means of post layout simulations to work with frequencies up to 55 MHz, across an extended temperature range $-40\text{ }^{\circ}\text{C} \div 125\text{ }^{\circ}\text{C}$, for supply voltages between $2.5\text{ V} \div 5.5\text{ V}$. Timing analysis also confirmed the timing performance for clock signals period of 18 ns and a setup time margin of at least 0.52 ns. This design targeted boosting the clock

frequency performance. The design was constrained for an 18 ns clock period. Internal sequential logic was designed for positive setup and hold times. For reaching high speed operation, logic cells with very small propagation delays were used. Another way contributing to achieving this performance was by the synthesis of the clock tree structure meant to distribute the clock equally to all leaf cells, thus enabling decreasing of skews and delays.

Preliminary defects analysis was performed on this controller. This analysis was done to obtain a first overview of how functionality of the block can be affected if internal structures have manufacturability issues. The results were obtained using special CAD tools dedicated to defects analysis on mixed signal integrated circuits, without requiring scan circuitry for evaluating the design. With one test, a number of 2218 defects were detected.

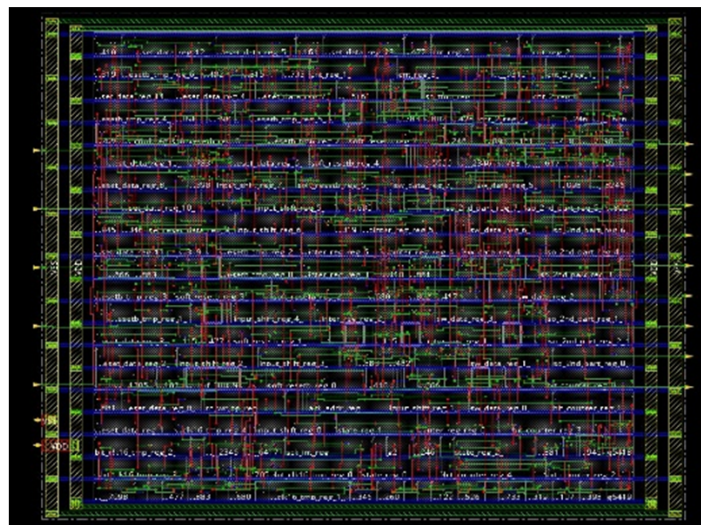


Fig. 3. Layout of the digital serial controller [7].

4. High Frequency Scan SPI Controller

Considering the general observations made in Section 2, the block proposed in [7] and described in Section 3, was redesigned for boosting its testability. For achieving this, scan circuitry was inserted. The resulted block can operate in two modes: user mode or test mode. The functional description provided in the previous section corresponds to the user mode.

When the circuit is in test mode, all flip-flops are forming one single shift register [17]. These flip-flops can be set to any value by shifting these values into the shift register. To observe the states of these flip-flops are observed by shifting their internal data out [17]. The scan flip-flops can be set or observed in a time which equals the number of flip-flops times clock period.

A diagram of the implementation is depicted in Figure 4, highlighting the main blocks comprised: the input pads, the output pads, the supply and ground pads, the SPI core and test controller structure. The circuit was implemented in a 65 nm CMOS technology.

Initially the digital core [7] consisted of one single block, the SPI core itself. For this self-test version (Fig. 5), the digital core contains two blocks, the SPI Core block, together with the TEST Controller added to detect the test mode entry sequence and to provide Test Mode input for the SPI Core. For Scan Enable input of SPI Core, it was considered an external port, actually a primary input of the chip.

The implementation of the scan design of SPI Core considered several rules [17]. Therefore, only data flip-flops (with reset) were used at synthesis, having role in design initialization. Primary Inputs/Outputs were assigned the following way: the SCK input of the chip serves as well as Scan Clock; the SI input serves as Scan Input, CSB pin serves as Scan Enable. Once test mode is detected, the test controller outputs a signal that is fed into the SPI Core. The SO pin is Scan Output. The clocks signals of the flip-flops used are directly controlled by the primary inputs.

The SPI Core (Fig. 4) is a block whose inputs are: Test_Mode and Scan_Enable, PENABLE, SCK, CSB, RESETB, and outputs are SO, Q[7:0] and sw_reset_data[15:0]. Its internal architecture is based on:

- the Finite State Machine whose states are: IDLE (at reset or at end of transaction) Register Address Identification, Read and Write.
- read/write operation identification structure,
- the input shifter that received the input data and outputs a group of eight bits
- bit counter
- SO-output data mechanism for handling the default SO code or for shifting the data out at read operations.
- index pointer for registers address handling
- the internal storage registers (four) and the reset configuration register.
- clock gating structure for power saving.

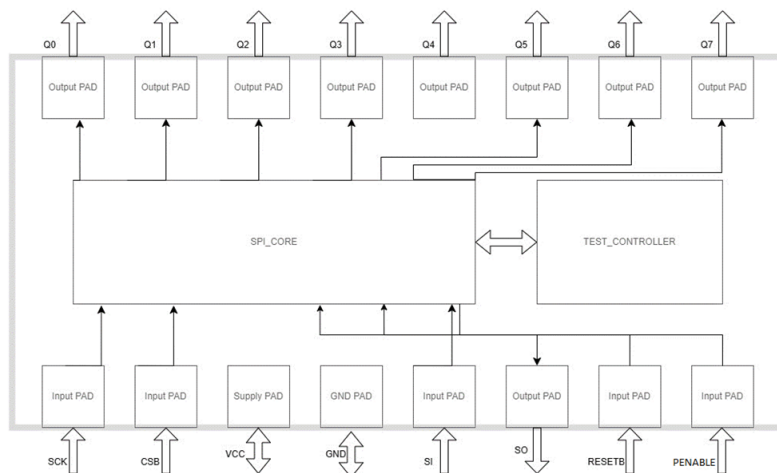


Fig. 4. Top level diagram of the SCAN SPI Controller chip.

These adjustments in the architecture targeted detection of stuck at 1/0 digital defects. Regarding the test mode entry and operation, a series of changes was implemented. Therefore,

serial data input/output is used as Scan Input/Output. The internal clocks signals used for registers update were multiplexed, such that in test mode ($\text{Test_Mode} = 1$) to copy the Scan clock. Software reset register is used for detecting the test mode entry command. When this command is detected, Test Mode signal is automatically asserted. Scan Enable signal was chosen to be an external signal: when ($\text{Test_Mode} == 1$), CSB pin can be used for transmitting the data from the exterior, otherwise this signal is kept low. The internal CSB signal is also multiplexed, in test mode it takes the values received on the line RESETB, otherwise in user mode it takes the value received from CSB pin.

5. Scan SPI Controller Implementation. Results

The floorplan of the chip is depicted in Figure 5, showing the placement of the pad structures, and the digital circuitry comprising SPI_CORE and TEST_CONTROLLER instances. As can be noticed, this is a pad limited design. The area which is unoccupied will be covered with filler cells. The layout of the entire circuit, comprising SPI Core, Test Controller and pad structures is depicted in Figure 5. A view of the layout of the digital circuits is offered in Fig. 6. The layout design considered the particularities of the low node technology that was used (65 nm CMOS) and succeeded in complying with all its rules.

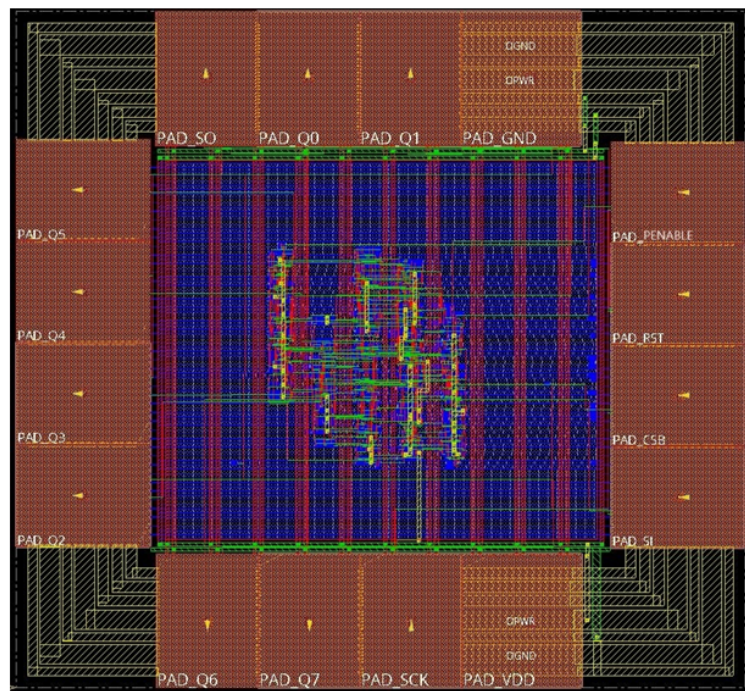


Fig. 5. Chip Floorplan.

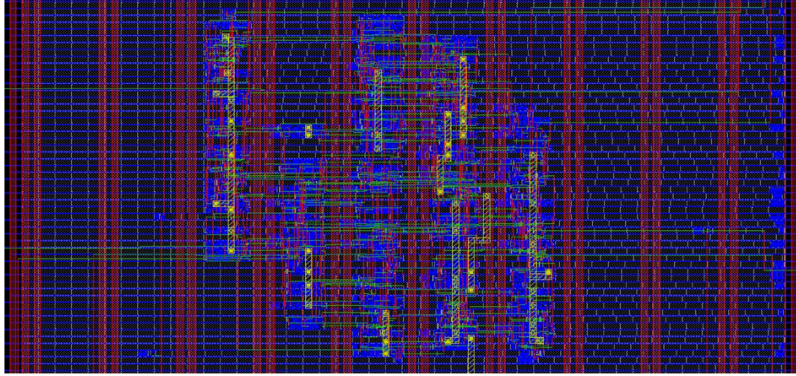


Fig. 6. Layout of the digital core.

In Table 1, there is provided a comparison between the initial implementation [7] and the self-test compliant implementation provided in this section. As it can be observed the functionality requirement remained the same, while this implementation has the advantage of being able to perform verifications on entire internal digital structure for manufacturing defects using only the inputs and the outputs of the chip. This controller was integrated with pad structures being able to form an entire chip, for which was targeted a QFN 16 leads package. The number of detected defects for the standard implementation, obtained by an indirect method, was 2218. The number of detected defects for SCAN SPI Controller is 2334. This analysis was performed using a specialized tool provided with the digital architecture containing the test mode circuitry. Of course, the advantages brought by the scan insertion come with a cost in utilized area. Since the layouts of the two were done on different platforms, a comparison in equivalent gates is provided. The standard design contained 811 equivalent gates whereas the second implementation has 4333 gates. For the SCAN SPI Controller, a value of 98.54% coverage was obtained.

Table 1. Comparison of Standard and SCAN SPI Controllers

Context	Standard SPI Controller [7]	Scan SPI Controller
Platform	CMOS 180 nm	CMOS 65 nm
Functionality	User Mode Read and Write Instructions Software Reset Command	User Mode Read & Write Instructions Software Reset Command Test Mode Detection \& Operation
Pinout	–	16 leads QFN package
Area [Equivalent Gates]	811	4333
Max. Freq. Operation	55	55
No. of defects	2218	2334
Coverage (digital)	–	98.54

Table 2 presents a synthesis of the results of defects analysis after the insertion of scan circuitry. As it can be seen, the estimate of coverage results after synthesis offered by the synthesis tool is 98.54%. The total number of faults is 2334, which 2006 are detected and 299 are likely detected, 1 is ATPG untestable and 28 are not detected. With a specialized TetraMax[®], DFT

tool, the coverage results are being confirmed. A number of 29 patterns were generated. The coverage number couldn't reach the value of 100% because of the design's small dimensions (as it is confirmed by the pad limited area being occupied by the digital circuitry) which led to impossibility of adjusting for testing few parts of it because of user mode functionality which had to be preserved.

Table 2. Defects Analysis Results

Context	Test Coverage [%]	Total faults
After Logical Synthesis	98.54	2334

Table 3 highlights the coverage results of this design compared with other similar works from literature which targeted digital circuits. Reference [18] shows comparable results with our work. As can be noticed, reference [19] is surpassed with about 6%.

Table 3. Test Coverage – Comparison with other papers

Context	Test Coverage [%]
This implementation	98.54
[7]	-
[18]	98.05
[19]	92.90

Figure 7 presents the waveforms corresponding to the input and output signals of the Scan SPI controller along with Test_Mode and Scan_Enable signals. These waveforms are obtained in Automatic Test Pattern Generation (ATPG) simulation. The output signal values corresponding to the input patterns propagated throughout the circuits are obtained. The obtained input and output vector will be used for ATE testing.

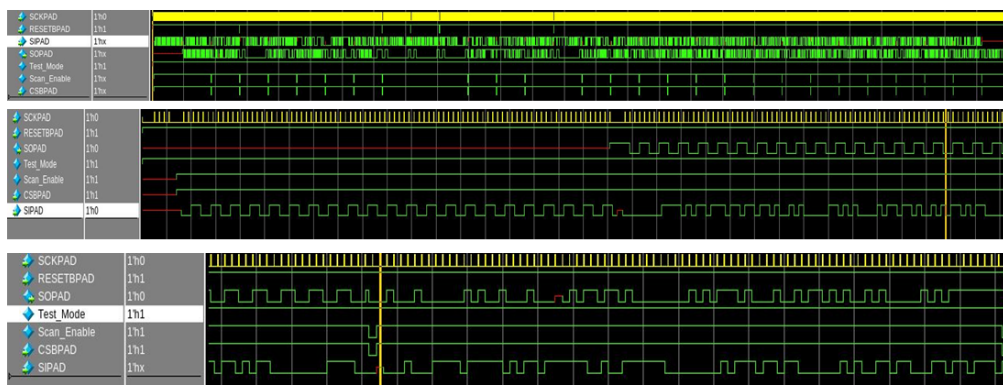


Fig. 7. ATPG simulations waveforms.

6. Conclusions

An improved SPI controller used in analog switches applications was designed in two architectures: the first one targeted serial functionality able to operate at 55 MHz and a second one derived from the previous, adjusted for testability reasons. For the second implementation, scan insertion was performed in order to adapt the initial architecture to a self-test capable version.

The improved SPI controller based on scan architecture was designed in a CMOS 65 nm technology. This design was validated through digital functionality simulations and timing analysis. The layout of the digital block was done and a top-level floorplan containing the input-output pad structures is implemented.

A coverage value up to 98.54% was obtained through extensive defects analysis done with custom synthesis and design for testability tools.

Further work targets design of other serial interfaces (e.g., I2C) with extended testability features.

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