ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY
Volume 28, Number 2, 2025, 119–124

Editorial: Special Issue on Topics in Semiconductors, Integrated Circuits, Sensors

Raluca MÜLLER[1, *] and Miron Adrian DINESCU[1]

[1]National Institute for Research and Development in Microtechnologies - IMT Bucharest Str. Erou Iancu Nicolae 126A, 077190 Voluntari, Ilfov, Romania

Email: raluca.muller@imt.ro*, adrian.dinescu@imt.ro

This special issue features a selection of 10 extended contributions of best papers from the International Semiconductor Conference (CAS 2024), as proposed by the conference chairpersons. The 47th edition of the International Semiconductor Conference – CAS 2024 (https://www.imt.ro/cas) brought together a strong scientific community who shared novel research results and discussed about challenges and solutions in the areas of nanoscience and nanoengineering, microsensors, microwaves, photonics, modelling, semiconductor devices and integrated circuits.

As one of the oldest conferences in Europe, started in 1978, CAS reflects advancements in the field, acting as a prestigious international platform and a catalyst for innovation in micro- and nanoelectronics. CAS 2024 took place from 9 to 11 October 2024, in the historical mountain resort of Sinaia, Romania. The conference was organized under the aegis of IEEE-EDS (Electron Devices Society) by the National Institute for Research and Development in Microtechnologies – IMT Bucharest, with the support of the Ministry of Research, Innovation and Digitalization. Since 1995, CAS has been an Institute of Electrical and Electronic Engineering (IEEE) event, being the largest international professional association in the world, which aims to stimulate technological innovation and excellence for the benefit of humanity.

CAS 2024 attracted 188 participants to the conference and the associated workshops, with 108 participants from Romania and 46 participants from 18 countries on four continents: China, Egypt, France, Germany, Greece, Israel, Italy, Kuwait, Poland, India, Iran, Ireland, The Netherlands, Serbia, Spain, Republic of Korea, UK, USA. The leading academic scientists, researchers, industry experts, and students attending the conference represented 54 organisations, 17 from Romania and 37 from abroad.

The conference featured a rich program comprising 3 plenary sessions with invited talks and 6 sessions for student papers, 2 poster sessions, workshops, exhibition, networking opportunities, Best Paper and Best Student Paper Awards, and enjoyable social events.

The technical program included 97 research papers, with 13 invited talks, 62 papers for oral presentations and 22 papers presented at the poster sessions. The original papers presented at the conference, were rigorously peer-reviewed and selected by the Technical Program Committee and the Paper Review Board. The best papers presented at the CAS 2024 conference were

awarded, 10 papers received the Best Paper Award, and 7 papers received the Best Student Paper Award, including two special awards and the "Dan Dascălu" award for the papers that received the maximum evaluation score.

The CAS 2024 conference successfully engaged industry, with contributions from companies like Infineon Technologies Romania and ON Semiconductor Romania, as well as international companies such as SILVACO (USA), Analog Power Conversion LLC (USA), STMicroelectronics Tours (France), and Melexis GmbH (Germany).

An exhibition showcasing services, products, and R & D projects took place for the whole conference duration, with relevant companies in the domain and national and international projects participating.

The CAS 2024 conference is an international forum, a highly collaborative environment, significantly strengthening the cooperation between recognized experts from academia and industry. The event provided great opportunities to be updated on the latest advances in micro- and nanotechnologies and semiconductors, addressing current topics of interest and challenges for the current and future development of this innovative field of science.

The first paper, "Measurement of Electromagnetic Feedthrough in Spin Wave Based Microwave Multiport Devices", authored by Alina-Cristina Bunea et al., in the Microwave & Millimeter Wave Circuits & Systems Section, describes the design, fabrication and experimental characterization of an RFID tag with electromagnetic wave polarization diversity operating in the 5 GHz frequency range. The tag implementation is based on two microstrip patch antennas with inset for impedance matching placed with the linear polarization in perpendicular direction. Between the antennas a circuit including a Schottky diode, as well as input and output matching networks is inserted and used for amplitude modulation (AM) of the received signal with the tag information. All the circuit blocks are fabricated using microstrip technology on the same FR-4 double clad substrate with a total area of 62×67 mm^2 and a thickness of 1.57 mm. The AM circuit block was modeled with the EM software package Mentor Graphics SSD (IE3D. The tag system was tested using rectangular and sinusoidal amplitude modulations and the experimental results validated the proposed concept in far-field conditions.

In the second paper, presented in the Modelling & Semiconductor Devices Section, entitled "Inclusion of Mechanical Stress Effects in a Compact MOSFET Model", by Nikolay Bonev et al., the authors extract the changes of various MOSFET parameters under the effect of mechanical stress. Because the analog performance of integrated circuits relies on stable parameters of its transistor and the mecanical stress changes the electronic properties of silicon and therefore, also the device parameters, the authors considered that a good model of these effects is needed for a predictable and reliable function of the circuits. The changes of various MOSFET parameters under effect of mechanical stress are extracted. A compact description of the stress effects is derived by applying tensors of piezo coefficients. They analyze the stress effects that occur in an IC after wafer production and before assembly, no strain engineering is involved. For the first time, the authors extracted the mobility and threshold voltages of MOSFETs with different orientations on a die using the EKV model in order to be able to integrate these direction- and stress-dependent model parameters into a circuit model. In conclusions are presented some rules to reduce the stress sensitivity in analogue circuits, based on the extracted coefficients, which can allow for stress correction in the EKV model which can support design and layout optimizations for minimal stress sensitivity in the most common usage of MOSFET in saturation mode.

In the third paper, "Circuit Techniques for Enhancing Output Current Accuracy in Floating Gate Drivers", Vlad Moise et al. presented in the Integrated Circuits I Section, two innovative

circuit techniques developed to dynamically compensate output current variations in high-voltage floating gate drivers. They can be efficiently used during both charge and discharge phases, significantly reducing the sensitivity of the output current to supply voltage fluctuations. The paper presents two novel architectures designed to improve output current precision. One method achieves this by adjusting the reference current, Iref, while the other compensates for variations by modifying the Ivgs current. The first method, referred to as Iref compensation, focuses on compensating the reference current and is applied exclusively in the VGS reference stage. The second proposed method, referred to as Ivgs compensation, is exclusively applied to the driving stage. The solutions effectively reduce the charge current error from 25% to 2%, showcasing their potential for improving the precision and reliability of gate drivers in practical applications. Due to their proven effectiveness in reducing charge current error, these methods are strong candidates for integration into future high-performance gate driver products.

In the fourth paper, presented in the Invited Papers Section, entitled "The Force Extraction Concept with application to Power IGBTs", the authors D. G. Sdrulla et al. condidered that the Insulated Gate Bipolar Transistor (IGBT) stands out as the most commercially advanced, seamlessly combining the high-input impedance MOS-gate control with the efficient bipolar current conduction that minimizes forward voltage drop, investigated the FE concept implemented on IGBT power devices (FE-IGBT). Firstly, an integrated FE-IGBT, for which the Extraction Plug and the Extraction Device (a lateral pMOS transistor with thick gate oxide) are built together on the same die. Secondly, a "hybrid" solution is proposed and explored, with the pMOS Extraction Deviceintegrated onto the freewheeling diode (FWD) instead. This paper is foccused on the validity of this approach and its benefits achieved by SPICE, TCAD and mixed-mode simulations and illustrates simulations and energy efficiency evaluations on a three-phase traction inverter for electric vehicles. Notable improvements in turn-OFF speed and energy efficiency, up to 40% during switching, are recorded. Simulations on a three-phase inverter automotive application with FE-IGBTs yielded spectacular efficiencies, over 98% at operating frequencies up to 25 KHz. The FE-IGBT has a significantly better trade-off between blocking and conduction performances, translating into a better technology curve. If properly implemented, this solution will revive the IGBT marked for the foreseeable future.

G. A. Bulzan et al. proposed in the fifth paper, "Separation of different orbital angular momentum photon states with log-pol transformation", presented in the Nanoscience & Nanophotonics Section, a logarithmic – polar component with its optical surface approximated by four discrete levels performs with a good approximation the same transformation of the optical vortices. Optical vortices (OVs) are diffraction patterns presenting a helicoidal wavefront in which the photon has an orbital angular momentum (OAM) that is equal to m where m is the order of the OV and is the reduced Plank constant. Their configuration is quite peculiar consisting on a donut-like shape with a hole in its center for m 6= 0. In the center point of an OV the phase is not defined. Due to the fact that the OAM of an OV is easily adjustable and the fact that the OAM can form an infinite Hilbert space, OVs have a wide range of applications in different domains. For instance, OAM can be used for coding and transmitting information in classical and quantum level. This paper showed theoretically, numerically and experimentally that an optical component with an optical surface discretized in four levels can perform a log – pol transformation. The optical pattern generated by an optical vortex diffracted by the log – pol component with four level is similar to the one generated by a log – pol component with a continuous surface. The numerical calculations and the experiment demonstrate that the contribution to the diffraction integral of the higher order Fourier terms is negligeable. This findings show that one can

significantly reduce the technological overhead in the process of manufacturing these log – pol optical components.

In the sixth paper, "Impact of Scaling and Interface Roughness on Drain Current in Nanosheet and Nanowire FETs: A 3D Monte Carlo Analysis", presented by M. G. K. Alabdullah et al., in the Sensors, Advanced Electronic Devices & Circuits Section, the authors investigated the impact of scaling gate length and oxide thickness, increase in source/drain doping concentration, and interface roughness on these architectures, which analyze the performance of nanosheet (NS) and nanowire (NW) field-effect transistors (FETs), which emerged as promising candidates for sub-3 nm CMOS technology. 3D finite-element Monte Carlo simulation toolbox, incorporating Schrodinger equation-based quantum corrections is performed. This simulation study explores strategies to enhance the electrical performance of n-type NS-FETs and NW-FETs at sub-2 nm technology nodes by examining the gate length scaling (LG), high-$\varkappa$ dielectric layer thickness, maximum doping concentration (MDC) in the source/drain (S/D) regions, and interface roughness (IR) between the channel and dielectric layer in order to meet the demands of sub-2 nm technology nodes. The auhors studied the impact of scaling gate length and oxide thickness, and changes in MDC and IR, on the performance of NS-FETs and NW-FETs, with a focus on optimizing the ON-current (IDD). Reduction in the high-$\varkappa$ dielectric layer thickness improved IDD in both devices, with a more pronounced effect in NS-FETs, particularly at LG = 10 nm. Higher n-type doping concentrations enhanced IDD, with NW-FETs benefiting more due to increased carrier injection from the highly doped S/D regions.

The seventh paper, "Design Space Exploration of Current-Starved Ring Oscillators Based on Graphene Nanoribbons", by F.-S. Dumitru et al., in the Nanoscience & Nanoengineering – Student Papers Section, presents an overview of related work on graphene, GNR conductance computation, GNR simulation methodology, logic circuits using GNRs, and current-starved oscillators. The authors describe the GNR-based current-starved oscillator concept, present the results of simulations for the GNR and FinFET oscillators and compares their performance. The authors investigated the potential of GNR devices to implement high-frequency ultra-low-power internal oscillators for multi-technology IC and explored the frequency range over which can be tuned the oscillator by driving the gate of the current source GNR-based device. The dynamic power consumption is reduced by applying the current starving technique to the ring oscillator topology. The proposed GNR-based design is compared with a 7nm Fin- FET counterpart and achieved a 1.89× higher output frequency while simultaneously reducing the power consumption by 553.8× and achieving a 812× higher power efficiency. A DSE of the frequency calibration and supply voltage is performed revealed that the GNR-based implementation achieves a 4.81× higher maximum output frequency and a 242× higher maximum power-efficiency when compared with the optimally configured FinFET implementation configured.

The eighth paper "An Area-Optimized Digitally-Assisted DAC Employing a Matrix-Based DEM Scheme", in the Integrated Circuits - Student Papers I Section, by A. Calinescu et al., presents a structured methodology for optimizing the DEM-assisted segmented DAC's area and details the proposed digital controller from a system-level perspectiveThe authors describe the system implementation together with a comparative analysis showcassing the DEM techniques advatages. High-resolution digital-to-analog converters (DACs) shape the audio systems high-fidelity (hi-fi). Unfortunately, component mismatch introduces nonlinearity, which degrades system performance. The proposed DAC system is implemented in a commercial 180nm CMOS process. The DEM controller is implemented using RTL description in SystemVerilog and synthesized to logic gates from the standard cell library of the aforementioned process using a com-

mercial synthesis solution for which TCL scripts have been developed. The digitally-assisted 9-bit segmented DAC, implemented, occupies an active area of 12999μm^2 and consumes up to 3.14mA from a 1.8V power supply at 400MHz. The maximum DNL and INL over 30 MC simulations and [-40°, 125°] temperature range are 0.75LSB and 0.57LSB, respectively, and 27/30 DACs have both their DNL and INL under 0.6LSB. Using the DEM engine renders the harmonics indistinguishable against the noise floor. This leads to an 8× improvement in SFDR and a 16× improvement in THD. The system achieves a THD of -79 dB and a SFDR of 79 dB.

The ninth paper, "First and Second Order Digital Circuits with Neuronal Models under Pulses Train Stimulus", by M. Popescu et al., was presented in the Modeling - Student Papers Section. The purpose of the paper is the simulation of flip-flop circuits using neurons, circuits which are considers as a promising topology. This paper extended the neuronal modeling from 0-order to 1-st and 2-nd order digital circuits. One or more neurons can be perceived as an analog circuit in terms of their voltage-time characteristics, but at the block level, they can rather fulfill a logic function. This later approach is imposed by the neuron membrane behavior that always works between two voltage levels – the resting potential and the acting potential, easily associated to two binary states. These levels change when an appropriate combination of pulses trains appears on the neuron's exciting and inhibiting input synapses. Being difficult to describe in all details the neuronal processes inside the human brain, this paper proposes some digital models able to mimic these biological processes. The first original element of this paper is the extension of the neuronal models, previously presented, from 0-order logic circuits to 1-order logic and 2-order logic circuits. The envelope signal shelters the pulses train that stimulate any neuron, and this envelope signal signature as the digital function represents an element of originality. The authors presented the simulation of an α-motoneurons pair stimulated to command an agonist-antagonist muscular pair and an alternative for the information storage within the central nervous system, knowing that every D latch or flip-flop can be used directly to memorize a bit of information.

The last paper of this Special Issue, "GaN Bootstrapped Logic Gates Analytical Modeling and Design Insights", authored by P. Medinceanu et al., was presented in one of the Integrated Circuits 1&2&3 Sections. The paper is focussed on the development of the GaN and the most commonly adopted logic gate topologies, because due to the variety of devices available in a monolithic GaN process, the development of digital circuits requires different topologies compared to CMOS technologies. The authors presented their results related to the analysis and design of logic gates from the bootstrapped (BS) family. Analytical equations for the static and dynamic parameters of an inverter are introduced. When compared to simulation results, these equations achieve a maximum error of 23.9% for static parameters and 33.3% for dynamic parameters. Additionally, different implementation details, such as developing other logic functions or enhancing the circuit behavior at system level, are proposed. The analysis of the static parameters of the GaN BS logic gates family is extended to dynamic parameters. The new approach for equations for dynamic parameters is validated by comparing the analytically calculated values with SPICE simulation results obtained using a Verilog-A-based device model.This method yielded a minimum error of 6.9% for tPHL and a maximum error of 33% for tF. Implementation practices, such as extending the INV design to NAND and NOR functions or incorporating further circuit enhancements, are proposed.

Acknowledgement. We would like to thank all the contributing authors, the reviewers and the Program Committee Members of CAS 2024 for their hard work, which contributed to the success of the conference. The Guest Editors would like to thank the Editor-in-Chief of the Romanian Journal of Information Science and Technology, Acad. Radu-Emil Precup and Acad.

Gheorghe Stefan, Honorary Co-Editor-in-Chief, for the publication of this special issue, which is very important for the visibility of the CAS conference and for IMT Bucharest.

We hope that the readers will find interesting the scientific contributions of this special issue in the fields of semiconductors, integrated circuits, sensors and nanotechnology.

June 2025

Dr. Raluca Müller - IMT Bucharest, and Dr. Miron Adrian Dinescu - IMT Bucharest, Guest Editors