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# Inclusion of Mechanical Stress Effects in a Compact MOSFET Model

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**Abstract.** The analog performance of integrated circuits relies on stable parameters of its transistors. Mechanical stress changes the electronic properties of silicon and therefore, also the device parameters. For circuit design a good model of these effects is needed for a predictable and reliable function of the circuits. This article extracts the changes of various MOSFET parameters under effect of mechanical stress. A compact description of the stress effects is derived by applying tensors of piezo coefficients. The deviations are included in the physically based compact EKV model. A comparison with measured data shows that the stress effects are modelled correctly within a 10 % error margin.

**Key-words:** EKV model; electron mobility; mechanical stress; MOSFET; parameter extraction; stress tensor; threshold voltage.

## 1. Introduction

Various internal and external forces cause mechanical stress on the silicon die. MOSFETs under such stress can have their physical and electrical parameters such as mobility and threshold voltages affected. External forces in particular can change after wafer fabrication due to assembly or soldering and need to be modelled to guarantee the circuit performance in the application [1].

The notion of strained layers has been in use since the early 1990s. There are a number of publications on strained layers that deal with the change in the band structure of the semiconductor [2]. Furthermore, models for the mobilities of electrons and holes in strained layers have been developed [3, 4]. Measurements have also been compared with simulations for MOSFETs [5].

In this paper we extend these theoretical models and add experimental analysis with data that can be fed back into circuit models. We analyse the stress effects that occur in an IC after

wafer production and before assembly, no strain engineering is involved. For the first time, we extract the mobility and threshold voltages of MOSFETs with different orientations on a die using the EKV model [6] in order to be able to integrate these direction- and stress-dependent model parameters into a circuit model.

The design of the test structures to measure stress effects on electronic devices is presented in section 2. In section 3. the physical effects of stress and strain on the electronic properties of silicon are discussed. The methodology to extract transistor model parameters is demonstrated in section 4. The measurement results for a test chip are presented and discussed in section 5.

## 2. Test Structure Design

In order to measure the parametric changes in the MOSFETs, a test chip was realized in a $0.18\,\mu\mathrm{m}$ SOI process with deep trench isolation (see Fig. 1). It comprises n- and p-channel MOSFETs of different sizes and orientations as well as other primitive devices and small circuits. Strips were cut out of the wafer (see Fig. 1) to apply a well defined stress by bending them on a four-point bending bridge (see Fig. 2). A force $F$ was applied on the inner supports through a spindle by setting a displacement $\Delta d$, where the inner supports are located symmetrically at the distance $L_i$ to the left and right of the die center. The force $F$ causes a moment between the inner supports which is constant and equal to $FL_o/2$ where $L_o$ is the distance between an inner and an outer support of the four-point bending bridge. As a result, an uniaxial stress $\sigma_{xx}$ occurs along the $x$-axis which varies linearly with $z$ reaching the maximal tensile value $\sigma_{xx_{max}}$ at the surface of the strip where the chip structures are formed. With the origin of the $z$-axis defined at its neutral zone in the middle of the strip and the strip thickness $t_{Si}$ there is $z = t_{Si}/2$ at the surface and $\sigma_{xx} = (2z/t_{Si})\sigma_{xx_{max}}$. The stress $\sigma_{xx}$ balances the moment between the inner supports leading to the following equation for a silicon strip of width $W_{Si}$ [7]:

$$W_{Si}\int_{-t_{Si}/2}^{t_{Si}/2}\sigma_{xx}z\,dz \;=\sigma_{xx_{max}}\cdot\frac{W_{Si}\cdot t_{Si}^2}{6} \quad=\quad \frac{F\cdot L_o}{2} \tag{1}$$

Then, the uniaxial stress component $\sigma_0$ in the direction of the strip can be computed by

$$\sigma_0 = \sigma_{xx_{max}} \quad=\quad \frac{3\cdot F\cdot L_o}{W_{Si}\cdot t_{Si}^2} \tag{2}$$

The orientation of the primitive components with respect to wafer flat is demonstrated in Fig. 1. The crystallographic orientation of wafer surface is [100] with flat orientation [110]. Orthogonal and diagonal strips were cut from the wafer to apply stress along the [110] and [100] directions respectively. The primitive devices are layouted in dedicated test cells in four different directions ($-45°$, $0°$, $45°$ and $90°$) to characterize different angles between the semiconductor lattice, the applied stress and the direction of current flow.

To eliminate errors due to mechanical hysteresis and non-elastic deformations, the displacement was swept four times, see Fig. 3. Because the parameter extraction is very sensitive to temperature changes, the temperature was measured by a PT100 and the temperature dependence of an on-chip resistor with a known small stress dependence.

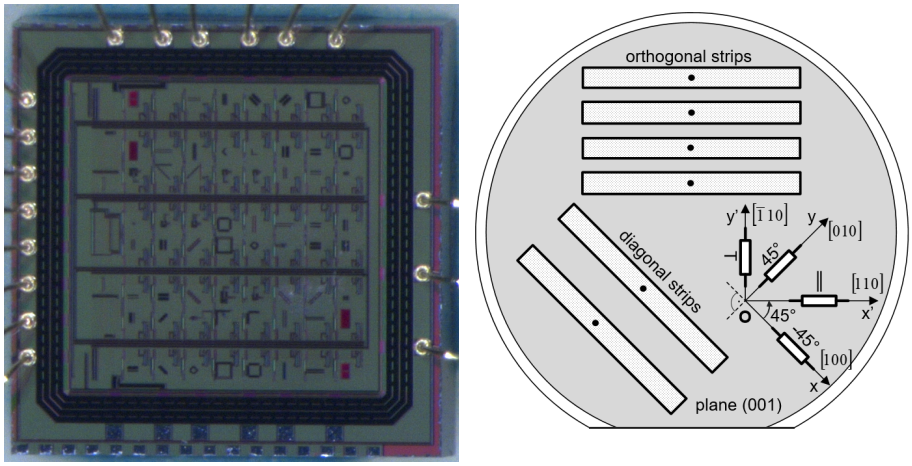


**Fig. 1.** Overview image of testchip with stress sensitive matrix of test structures and orientations of primitive components and silicon strips on silicon wafer.

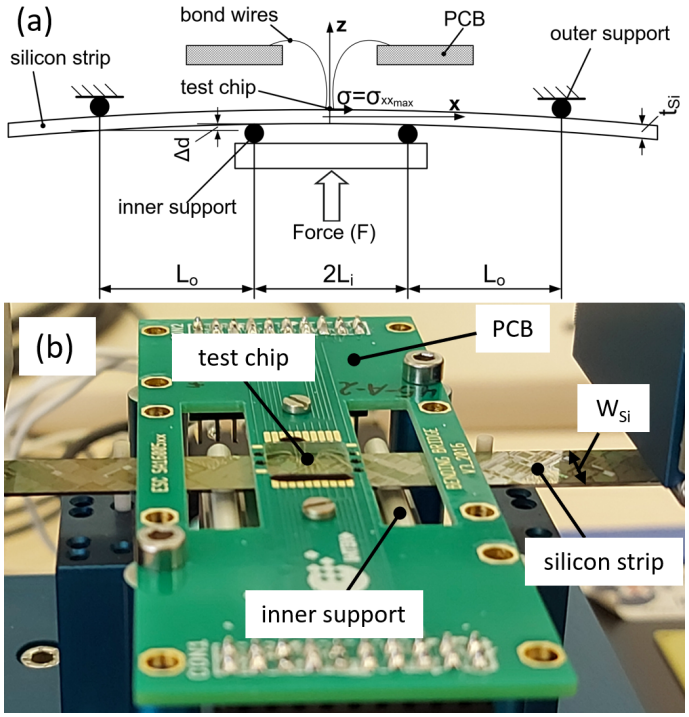


**Fig. 2.** (a) Principle of operation of the four-point bending bridge. (b) Top view of the silicon strip with the wire bonded test chip and the PCB.

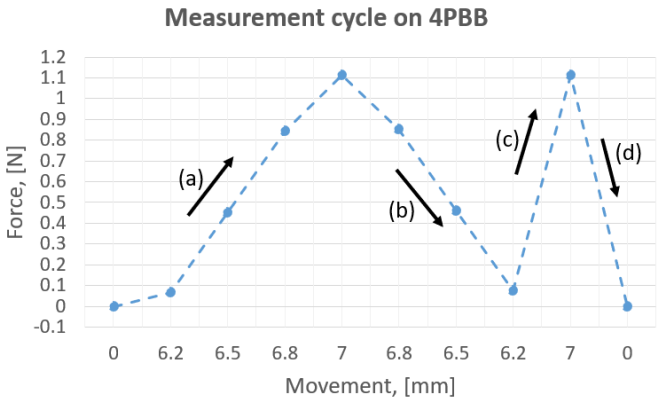


**Fig. 3.** Sweeps of the z-stage movement during a typical measurement cycle on the four-point bending bridge setup (4PBB). Movement $0\,\mathrm{mm}$ corresponds to the stress free condition.

# 3. Strain in Silicon

Stress describes internal forces of a body that can result from forces applied to the body from outside (external stress) or from material properties (internal stress). In this paper we only discuss the effects of external stress. Stress causes strain in the substrate of the silicon material. The strain then leads to a change in the physical properties of the silicon and reduction of its crystal cubic symmetry [8], [9]. According to Chidambaram [10] stress is the cause of strain in the material and the following material properties change or alter with strain:

- The band structure of a material,
- therefore the band gap and the effective mass of electrons and holes are changed,
- the equilibrium carrier densities change because of the change of the effective masses,
- with change of effective masses changes the mobility and the mobility becomes an-isotropic,

The equilibrium densities of electrons and holes $n_0$ and $p_0$ are of particular interest for the analytical description of electronic devices. The density of states can be used to determine the equilibrium charge densities and the intrinsic density. Furthermore, the flatband voltage of a MOS-capacitor is affected if the bandgap and the conduction and valence band edges are shifted. This causes a change in threshold voltage which has to be investigated as well.

# 4. Measurement and Extraction of the Stress Related Parameters

## 4.1. Simplified EKV model equations

The extraction of the stress related parameters should rely on a physically based MOSFET model because the transistors are biased in all regions (weak, moderate and strong inversion). Therefore,

the simplified EKV model was chosen as a reference model. The current is given by:

$$I_D = I_s \cdot \left[ ln^2 \left\{ 1 + \exp\left( \frac{V_p - V_{SW}}{2 \cdot U_T} \right) \right\} - ln^2 \left\{ 1 + \exp\left( \frac{V_p - V_{DW}}{2 \cdot U_T} \right) \right\} \right] \tag{3}$$

In this equation $V_{SW}$ and $V_{DW}$ are the source and drain voltages related to the local substrate, $U_T = kT/q$ is the temperature voltage and $V_P$ is the pinch-off voltage where the inversion channel is pinched off for a gate voltage $V_{GW}$. The pinch-off voltage is given by:

$$V_p = \frac{V_{GW} - V_{T0}}{n} \tag{4}$$

where $n = [\frac{\partial V_P}{\partial V_G}]^{-1}$ is the slope factor, which is assumed constant in our investigation. The specific current $I_s$ is given by:

$$I_s = 2 \cdot n \cdot U_T^2 \cdot \mu_0 \cdot C_{ox} \cdot \frac{W}{L} = I_0 \cdot \frac{W}{L} \tag{5}$$

where $\mu_0$ is the mobility of the carriers in the inversion channel and $C_{ox} = \epsilon_0 \cdot \epsilon_{SiO_2}/T_{ox}$ is the specific gate capacitance per unit area. The capacitance is dependent on the oxide thickness $T_{ox}$.

Is is not as simple to calculate the sensitivity of the mobility and the threshold voltage, because the applied stress causes strain in the silicon. Strained silicon shows significant changes in electronic material properties, for instance the effective longitudinal and transversal masses, the bandgap $E_G$, and the effective density of states change under strain. The mobility gets anisotropic and changes its value depending on the components of strain tensor.

Therefore, it is necessary to extract the threshold voltage $V_{T0}$, the mobility $\mu_0$ and the slope factor from measurements separately. The EKV model extracts the threshold voltage for a constant current $I_D = I_s/2$. In this case the constant current is not chosen arbitrarily like for other models.

The extraction is outlined in [11] and [6] for a more generalized approach. A first measurement determines the specific current $I_s$ and a second measurement finds the threshold voltage $V_{T0}$ and the slope factor $n$.

The specific current is derived from the slope $m$ of $\sqrt{I_D}$ when sweeping the source voltage $V_{SW}$ (see Fig. 4):

$$I_s = (m \cdot 2 \cdot U_T)^2 \text{ with } m = \min\left( \frac{\partial \sqrt{I_D}}{\partial V_{SW}} \right) \tag{6}$$

The ratio between the drain- and the specific current is called inversion coefficient $IC = I_D/I_s$ and defines the operation range of the transistor. If $IC < 0.1$, the transistor is in weak inversion, between $0.1 < IC < 10$ the transistors is in moderate and for $IC > 10$ in strong inversion. The current $I_s$ is dependent on strain in the silicon because the mobility changes with strain. If the transistor is operated in strong inversion the second term in Eq. (3) is very small and can be neglected. Under this condition, the equation for the pinch off voltage simplifies to

$$V_P = V_{SW} + 2 \cdot U_T \ln\left[ \exp\left( \sqrt{\frac{I_D}{I_s}} \right) - 1 \right] \tag{7}$$

The second term in Eq. (7) is zero if the transistor is biased at $I_D = I_s \left(\ln(2)\right)^2 \approx I_s/2$ as shown in Fig. 5. For our test setup it was not possible to bias the transistor with very low currents.

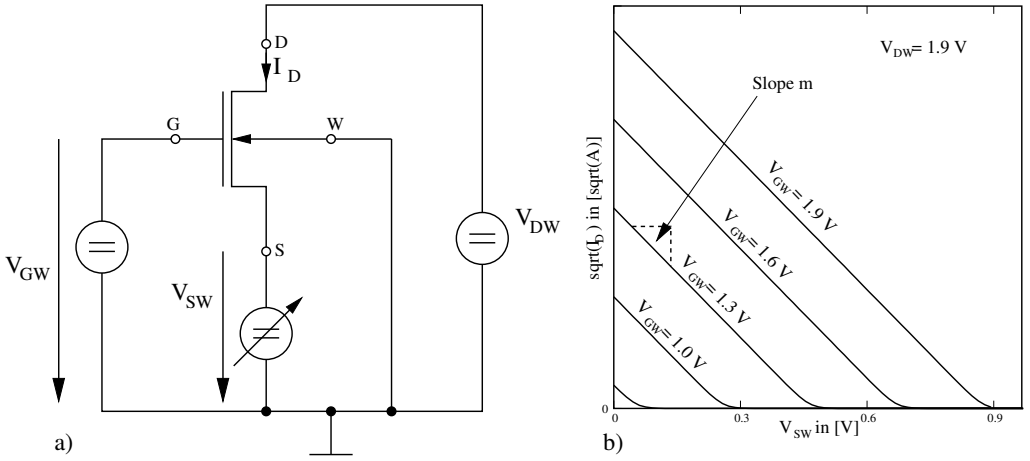


**Fig. 4.** Extraction setup for the specific current $I_s$

Therefore, higher currents were applied as shown in [6] resulting in IC between 12 and 15 and the second term of Eq. (7) being the correction term. Such inversion coefficients are only slightly above the onset of strong inversion, hence the vertical high-field effects can still be considered minimal. The threshold voltage can be found from Eq. (4) and (7) from

$$V_{SW} + 2 \cdot U_T \ln \left[ \exp \left( \sqrt{\frac{I_D}{I_s}} \right) - 1 \right] = \frac{V_{GW} - V_{T0}}{n} \tag{8}$$

The source voltage $V_{SW}$ is set to the negative correction term. Then, the left side of Eq. (8) is zero and $V_{GW} = V_{T0}$. The drain source voltage was set to a constant value of $V_{DS} = 0.2\,\mathrm{V}$ to avoid velocity saturation at the drain side of the transistor. The slope factor $n$ is the inverse of the slope of the function $V_{SW} = f(V_{GW})$ at the cross point with the $x$-axis.

Now it is possible to calculate the mobility from the $n$-factor and the previously extracted specific current as follows:

$$\mu_0 = \frac{I_s}{2 \cdot n \cdot U_T^2 \cdot C_{ox} \cdot \frac{W}{L}} \tag{9}$$

The extraction method is very sensitive to the temperature because the $I_s$ depends on $\sim U_T^2$. So it was necessary to monitor the temperature with two sensors (external PT100 and an internally temperature calibrated resistor with a very low stress dependence).

## 4.2. Piezo coefficients

The model parameters have different stress sensitivities in each spacial direction. Therefore, the model parameters depend on the device orientation $\vec{l}$ which we define as a unit vector pointing from the source to the drain of the transistor. We model the direction dependency by a symmetrical second rank tensor [12]. For the mobility there is

$$\mu(\vec{l}, \sigma) = \mu_0 \cdot \left( 1 + \vec{l}^{\mathsf{T}} \cdot M(\sigma) \cdot \vec{l} \right) \tag{10}$$

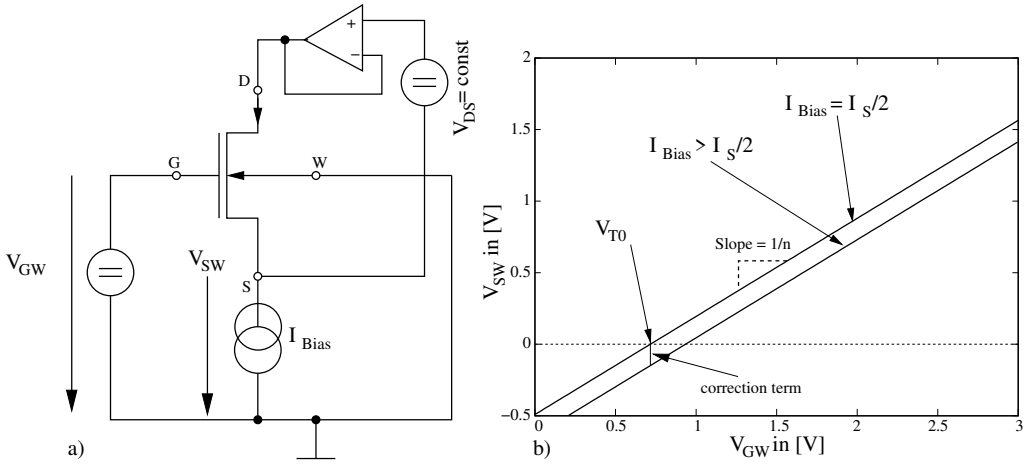


**Fig. 5.** *Threshold voltage extraction setup*

where $M$ is the stress dependent tensor of relative mobility variations and $\mu_0$ is the mobility of the stress free transistor. The dependence of $M$ on the stress tensor $\sigma$ is given by the 4[th] rank tensor $\Pi_M$ of mobility piezo coefficients.

$$M(\sigma) = \Pi_M \cdot \sigma \tag{11}$$

The mobility variations $M = (m_{ij})$ and the stress tensor $\sigma = (\sigma_{ij})$ $(i, j = 1, 2, 3)$ are symmetrical, therefore they have 6 different components and the tensor of piezo coefficients $\Pi_M = (\mu_{mn})$ $(m, n = 1 \ldots 6)$ has 36 different components. Because of crystal symmetry only 4 of these, $\mu_{11}$, $\mu_{12}$ and $\mu_{44}$, are independent [12]. With a coordinate system along the principal crystal axes this can be written as

$$\begin{pmatrix} m_{11} \\ m_{22} \\ m_{33} \\ m_{12} \\ m_{13} \\ m_{23} \end{pmatrix} = \begin{pmatrix} \mu_{11} & \mu_{12} & \mu_{12} & 0 & 0 & 0 \\ \mu_{12} & \mu_{11} & \mu_{12} & 0 & 0 & 0 \\ \mu_{12} & \mu_{12} & \mu_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \mu_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \mu_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \mu_{44} \end{pmatrix} \cdot \begin{pmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{12} \\ \sigma_{13} \\ \sigma_{23} \end{pmatrix} \tag{12}$$

The components $\mu_{ij}$ of the stress tensor can be determined by extracting the model parameters of transistors with similar geometry at various orientations and stress conditions. Each extraction of the mobility $\mu(\vec{l}, \sigma)$ for a transistor with orientation $\vec{l}$ at stress $\sigma$ gives a linear constraint for the components of the piezo tensor $\Pi_M$. Because in our extraction, all devices are lateral and stress is only applied in $x$ and $y$ directions, there is

$$\vec{l} = \begin{pmatrix} l_x \\ l_y \\ 0 \end{pmatrix} \text{ and } \sigma = \begin{pmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{12} & \sigma_{22} & \sigma_{23} \\ \sigma_{13} & \sigma_{23} & \sigma_{33} \end{pmatrix} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} & 0 \\ \sigma_{xy} & \sigma_{yy} & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{13}$$

Substituting this into Eq. (12), (11) and finally (10) results in

$$\mu(\vec{l}, \sigma) = \mu_0 \cdot \left(1 + \mu_{11}\left(l_x^2\sigma_{xx} + l_y^2\sigma_{yy}\right) + \mu_{12}\left(l_x^2\sigma_{yy} + l_y^2\sigma_{xx}\right) + \mu_{44} \cdot 2 l_x l_y \sigma_{xy}\right) \tag{14}$$

**Table 1.** Extracted parameters for different rotation angles ($d = \sqrt{2}/2$)

| Strip | $\gamma$ | $\sigma_{xx}$ | $\sigma_{yy}$ | $\sigma_{xy}$ | $l_x$ | $l_y$ | $\frac{\Delta\mu}{\sigma\mu_0}[\frac{1}{\mathrm{GPa}}]$ | $\frac{\Delta V_{T0}}{\sigma}[\frac{\mu\mathrm{V}}{\mathrm{GPa}}]$ | $\frac{\Delta n}{\sigma n_0}[\frac{1}{\mathrm{GPa}}]$ |
|---|---|---|---|---|---|---|---|---|---|
| orth. | 90 | $\sigma_0/2$ | $\sigma_0/2$ | $\sigma_0/2$ | $-d$ | $d$ | 0.120 | -23.4 | -0.001 |
| orth. | 45 | $\sigma_0/2$ | $\sigma_0/2$ | $\sigma_0/2$ | 0 | 1 | 0.318 | -14.4 | -0.005 |
| orth. | 0 | $\sigma_0/2$ | $\sigma_0/2$ | $\sigma_0/2$ | $d$ | $d$ | 0.552 | -4.8 | -0.010 |
| orth. | -45 | $\sigma_0/2$ | $\sigma_0/2$ | $\sigma_0/2$ | 1 | 0 | 0.320 | -14.0 | -0.005 |
| diag. | 90 | $\sigma_0$ | 0 | 0 | $-d$ | $d$ | 0.336 | -10.8 | -0.006 |
| diag. | 45 | $\sigma_0$ | 0 | 0 | 0 | 1 | 0.198 | -6.5 | -0.015 |
| diag. | 0 | $\sigma_0$ | 0 | 0 | $d$ | $d$ | 0.338 | -11.4 | -0.005 |
| diag. | -45 | $\sigma_0$ | 0 | 0 | 1 | 0 | 0.448 | -15.8 | 0.004 |

A similar dervation for the threshold voltage gives

$$V_{T0}(\vec{l},\sigma) = V_{T00} \cdot \vec{l}^{\intercal} \cdot \Pi_V \cdot \sigma \cdot \vec{l} \tag{15}$$

where $\Pi_V = (\nu_{mn})$ $(m,n = 1 \ldots 6)$ denotes tensor of piezo coefficients for the absolute threshold voltage change over the threshold voltage $V_{T00}$ of the stress free transistor. The constraints for the piezo coefficients $\nu_{11}$, $\nu_{12}$ and $\nu_{44}$ become

$$V_{T0}(\vec{l},\sigma) = V_{T00} + \nu_{11}\left(l_x^2\sigma_{xx} + l_y^2\sigma_{yy}\right) + \nu_{12}\left(l_x^2\sigma_{yy} + l_y^2\sigma_{xx}\right) + \nu_{44}\cdot 2 l_x l_y \sigma_{xy} \tag{16}$$

Once the piezo coefficients are known, the model parameters can be computed for devices with arbitrary orientation $\vec{l}$ and stress $\sigma$ by Eq. (10) and (15).

# 5. Extraction Results

The changes of the threshold voltage $V_{T0}$, the mobility $\mu$ and the slope factor $n$ due to stress were extracted from four different layouts of a $1.8\,\mathrm{V}$, long channel n-MOSFET device of size $W/L = 10\,\mu\mathrm{m}/50\,\mu\mathrm{m}$ for the orthogonal and the diagonal strips. These layouts are denoted by their angle between the wafer flat and the direction of current flow from source to drain at $-45°$, $0°$, $45°$ and $90°$ respectively. The components of the stress tensors and the device orientations are shown in Table 1 for the coordinate system along the principal crystal axes $x$ and $y$ (see Fig. 1). The main stress component $\sigma_0$ was derived from the applied force $F$ by Eq. (2) . The stress tensor components for the orthogonal strip result from a $\phi = -45°$ rotation of the tensor $\sigma' = (\sigma'_{xx} = \sigma_0)$ around the $z$-axis [13]

$$\begin{array}{rcrcrcl} \sigma_{xx} & = & \sigma'_{xx}\cos^2(\phi) & = & \sigma'_{xx}/2 & = & \sigma_0/2 \\ \sigma_{yy} & = & \sigma'_{xx}\sin^2(\phi) & = & \sigma'_{xx}/2 & = & \sigma_0/2 \\ \sigma_{xy} & = & -\sigma'_{xx}\sin(\phi)\cos(\phi) & = & \sigma'_{xx}/2 & = & \sigma_0/2 \end{array} \tag{17}$$

For the orthogonal and the diagonal strips, we varied the stress magnitude as hysteresis sweep (see Fig. 3) and extracted the device parameters. There is a good linear dependency of the relative mobility variation $\Delta\mu/\mu_0$ and the threshold variation $\Delta V_{T0}$ with respect to the stress up to the maximum applied stress of $60\,\mathrm{GPa}$ (see Fig. 6 and 7). For the orthogonal strip, the $-45°$ and $45°$ layouts have similar sensitivities due to the crystal symmetry, The same holds for the $0°$ and $90°$ layouts of the diagonal strip.

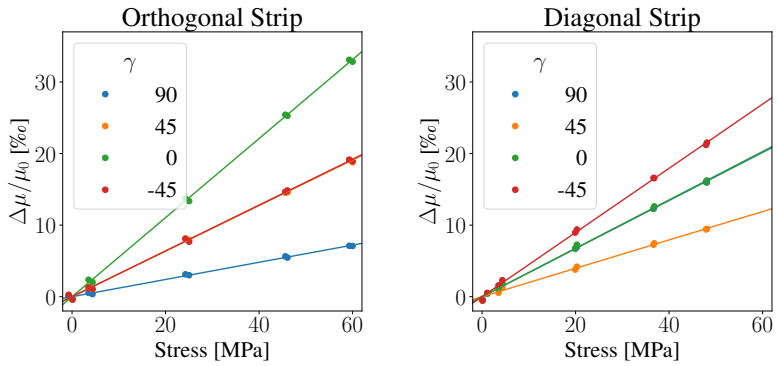


**Fig. 6.** Extracted relative changes of the mobilities over stress for the orthogonal strip (left) and the diagonal strip (right). Dots are measured values, lines are best linear fits.

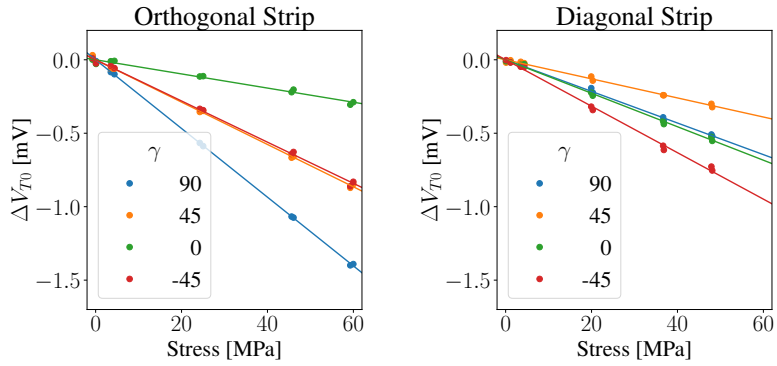


**Fig. 7.** Extracted changes of the threshold voltage $V_{T0}$ over stress for the orthogonal strip (left) and the diagonal strip (right). Dots are measured values, lines are best linear fits.

**Table 2.** Extracted piezo coefficients. $E$ is the square root of the mean square error.

| Index $ij$ | $\mu_{ij}$ [$\mathrm{GPa}^{-1}$] | $\nu_{ij}$ [$\frac{\mu\mathrm{V}}{\mathrm{GPa}}$] |
|---|---|---|
| 11 | 0.45 | -17.3 |
| 12 | 0.20 | -8.0 |
| 44 | 0.43 | 18.6 |
| $E$ | 0.002 | 1.5 |

The linear dependency between stress and model parameters demonstrates a constant stress sensitivity of these parameters computed from the slope of the linear fit. The stress sensitivity was also extracted for the slope factor $n$ (not depicted in a diagram) showing that it is almost stress independent (see Table 1).

The stress sensitivities for the mobility and threshold can now be applied determine the piezo tensors for these values by Eq. (10) and (15) resulting in 8 constraints (one per row of Table 1) for the three piezo coefficients. We solved these over constrained systems of equations for the least square errors (see Table 2). The different signs compared to [14] result from a different choice the the coordinate system. Changes in the magnitude of the piezo coefficients are caused by now including all measurements, increasing the accuracy, while [14] only included the parameters of three devices. The error $E$ (square root of the mean square error of the solution) gives an indication on the validity of the methodology. While the error is less than 0.5 % (with respect to the biggest component) for the mobility, it is 10 % for the threshold voltage, presumably because of the bigger uncertainty of the threshold voltage extraction, measured at very small currents in the range of $I_s$.

For both strips the stress sensitivity of the mobility is the biggest when the current flows parallel to the stress ($0^\circ$ for the orthogonal and $-45^\circ$ for the diagonal strips) and is the smallest when the current flows perpendicular to the stress. Furthermore, the stress sensitivity is bigger for stress in the 110 crystal direction (the orthogonal strip, along the wafer flat) than for the 100 crystal direction (the diagonal strip).

Notably, for the orthogonal strip, the stress sensitivity of the threshold voltage is bigger for the stress orthogonal to the current flow and it becomes the smallest when the stress is parallel to the current flow. This is not the case for the diagonal strip where the threshold voltage sensitivities behave similar to these of the mobility. As with the mobility, the threshold voltage sensitivity in 110 crystal direction is bigger than in 100 crystal direction.

## 5.1. Stress sensitivity in the EKV model

For the characterized devices, an EKV model was extracted in the stress free state and compared to measured data (see Fig. 8 left). Then, the extracted stress dependencies were added to the model. The modified model was verified by comparing it to measured data at different stress magnitudes.

The extracted long channel EKV model with stress dependent mobility and threshold voltage shows a good agreement with the measurements for the stress free case and it also models the stress dependence with an accuracy of 10 % for the drain current $I_D$ (see Fig. 8 right).

It was shown that the threshold voltage changes with out of plane stress [15]. Our work quantifies the dependency between stress and threshold voltage for in plane stress. This is also confirmed by the increasing stress sensitivity with the decreasing gate source voltage (see Fig. 8).

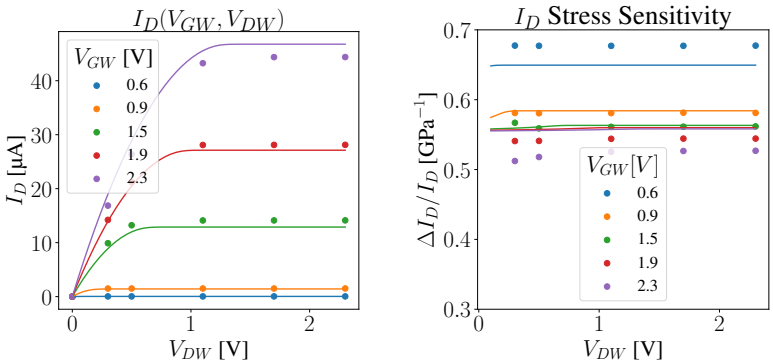


**Fig. 8.** Comparison between the measurements (dots) and the EKV model (lines) for the output characteristics and its stress sensitivity of the MOSFET at the orthogonal strip with $\gamma = 0°$

The threshold voltage $V_{T0}$ decreases with stress. This is because the bandgap $E_G$ and the effective density of states $N_V$ decrease with strain [4]. Both values determine the flat-band voltage of the MOSFET significantly.

The stress dependence of the threshold voltage implies that circuits become more sensitive to stress effects if biased close to the threshold voltage.

Because the results were obtained for long channel devices, it is expected that these results are relevant for all transistor geometries without short-channel effects.

## 6. Conclusions

This paper demonstrates the extraction of piezo coefficients for the mobility and threshold voltage of the EKV model. The extracted coefficients can then allow for stress correction in the EKV model which can support design and layout optimizations for minimal stress sensitivity in the most common usage of MOSFET in saturation mode.

To reduce the stress sensitivity in analogue circuits the following rules can be followed:

- Considering stress along the major crystal axes 100 and 110, the current flow direction should be perpendicular to the stress. This reduces the stress sensitivity of the mobility by more than a factor of two.

- The gate overdrive voltage should be sufficiently large to suppress stress effects because the previous rule is not always valid for the threshold voltage.

- The stress sensitivity is smaller in the 100 crystal axis compared to the 110 axis.

With the same methodology the stress dependence can be extracted for short-channel devices, other temperatures and p-channel MOSFET devices in future work.

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