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Design and Simulation of Integrated Radio Frequency Transmitter for Wireless Sensor Network Applications

Zhenyao LI[1,2], Jie JIN[1,*], Daobing ZHANG[2], and Zhijing LI[3]

[1]School of Information Engineering, Changsha Medical University, 410219 Changsha, China
[2]Sanya Institute of Hunan University of Science and Technology, Sanya, 572024 Hainan, China
[3]School of Information and Electrical Engineering, Hunan University of Science and Technology, Xiangtan, 411201 Hunan, China
Email: lizhenyao@mail.hnust.edu.cn, jj67123@hnust.edu.cn*, dbzhang@hnust.edu.cn, lizhijingwei@hnust.edu.cn.
* Corresponding author

Abstract. This paper introduces a low-voltage low-power integrated radio frequency (RF) transmitter using GlobalFoundries' 0.18 μm CMOS RF process technology for 2.4 GHz wireless sensor network (WSN) applications. The proposed RF transmitter consists of an LC voltage-controlled oscillator (VCO) and a sub-harmonic mixer. The VCO utilizes an LC tank to achieve reduced phase noise and enhanced frequency stability, the sub-harmonic mixer is optimized for lower power consumption and reduced harmonic distortion, addressing limitations observed in previous designs, and the collaboration between the VCO and the sub-harmonic mixer ensures that the RF transmitter operates stably and efficiently. Simulation experiments demonstrate that the integrated RF transmitter operates effectively at 1V supply voltage, and its power consumption is 2.55 mW, showcasing its suitability for low-power applications typical in WSNs where energy efficiency is critical. In terms of linearity, the input-referred third-order intercept point (IIP3) of the transmitter reaches 3.19 dBm, which exhibits its ability to handle third-order nonlinearities and robustness against interference. Additionally, the RF transmitter achieves a conversion gain of approximately 12.5 dB, which demonstrates its effectiveness in signal amplification and ensures that the transmitter is capable of providing sufficient power to the received signals, enabling reliable applications in WSNs.

Key-words: Complementary metal-oxide-semiconductor (CMOS); mixer; oscillator; radio frequency (RF); transmitter; wireless sensor network (WSN).

1. Introduction

Wireless sensor networks (WSNs) have attracted considerable attention in recent years owing to their affordability, adaptability and extensive application domains [1-3]. As fundamental components of WSN, RF receivers and transmitters facilitate the transmission and reception of RF signals, thus determining the overall efficiency and performance of the system. The block diagram of an RF transmitter for WSN is depicted in Fig. 1. In this configuration, intermediate frequency (IF) signals are initially filtered to remove high-frequency interference through a low-pass filter (LPF), and these filtered IF signals are later converted into RF signals by a mixer and a voltage-controlled oscillator (VCO). The converted RF signals are further amplified by a power amplifier (PA) and refined by a band pass filter (BPF) to remove unwanted frequency components before being emitted by the antenna [4–7]. This diagram underscores the critical role of the mixer and VCO as indispensable components in the WSN RF transmitter.

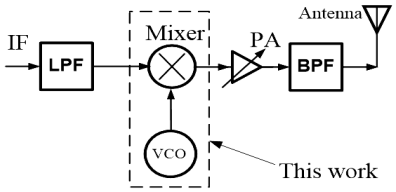

Fig. 1. Block diagram of RF transmitter in WSN.

With the rapid development of semiconductor technology and the increase in chip operating frequencies, the power consumption of chips has rapidly increased, and the increase in power consumption lead to an increase in chip heat generation and a decrease in reliability. Therefore, power consumption has become an important consideration in deep submicron integrated circuit design [8–11]. The advancement of microelectronics technology has facilitated the widespread adoption of highly integrated and low-cost CMOS RF transceiver IC in industrial and consumer electronics, and effectively reduced the power consumption of RF chips. In 2006, Nguyen et al. [12] proposed a low-power RF transceiver front-end using 0.18-μm CMOS technology for the IEEE 82.15.4 standard in the 2.4 GHz frequency band. The RF receiver includes a single ended low noise amplifier, a four quadrant passive mixer, and a transimpedance amplifier. The test results indicate that the receiver and transmitter front-end respectively consume 3.5 mA and 3 mA under a power supply of 1.8 V. In 2022, Li et al. [13] designed and manufactured a 1.15 mW 3.75-4.25 GHz frequency modulated broadband transmitter using a 65 nm CMOS process. The transmitter features digitally reconfigurable carrier frequencies and ultra wideband RF bands. In 2023, Pour et al. [14] proposed a low-power, low complexity direct digital to RF transmitter architecture suitable for biosensing applications. The simulation results show that the transmitter consumes less than 0.5 mW power consumption. In 2024, An et al. [15] proposed a fully digital, crystal free pulse radio ultra wideband transmitter that achieved a data transmission rate of 1.8 Gbps with a power consumption of only 4.09 mW.

Subharmonic mixer performs harmonic mixing of RF signal and local oscillator (LO) signal, and it can improve the DC drift problem of zero IF receivers [16–18]. In 2016, Jin [19] proposed a subharmonic mixer based on a low-voltage low-power resonant amplifier, which adopts current reuse and discharge technology and is suitable for zero intermediate frequency transceiver system applications. In 2017, Seydhosseinzadeh et al. [20] proposed a broadband Gilbert subharmonic

mixer that partially overcomes the fundamental trade-off between RF and IF currents. In 2023, He et al. [17] proposed a novel mixer with reduced size, which achieved U-band subharmonic mixer through 0.15 μm GaAs pHEMT process. In 2023, Gaurav et al. [21] proposed a millimeter wave subharmonic mixer using a stacked double balanced Gilbert cell topology. This circuit applies source degradation configuration to LO input and RF input to achieve high linearity.

The presented CMOS RF transmitter integrates a VCO and a mixer, forming a compact and efficient architecture tailored for WSN applications. The VCO employs a stacked NMOS and PMOS transistor configuration that leverages their complementary behaviors to generate a robust negative resistance [22-24]. This negative resistance compensates for losses in the LC tank circuit, ensuring sustained oscillations and low phase noise. Using a passive LC tank, the VCO achieves precise frequency control, producing two sinusoidal signals with a 180° phase difference - critical for driving the mixer stage [25, 26].

The mixer adopts a subharmonic approach, in which the second harmonic of the LO signal is utilized for mixing [27]. This reduces the required LO frequency by half, effectively reducing power consumption and easing the design constraints on the VCO. This innovative approach not only enhances power efficiency but also enables higher levels of system integration, making the transmitter ideal for energy-constrained WSN nodes.

The proposed architecture offers substantial benefits compared to traditional RF transmitters. By integrating the VCO and mixer into a single CMOS-based module, the design achieves remarkable reductions in power consumption and circuit complexity [25]. The stacking transistor configuration in the VCO minimizes the noise contributions of active devices while maximizing energy efficiency, addressing critical challenges in the design of RFIC [26].

This paper is structured as follows. In Section 2, the schematic diagram of the LC VCO and its simplified AC equivalent circuit are presented. Moreover, the phase noise of the LC VCO is analyzed, and then the functionality of the sub-harmanic mixer used in the WSN transmitter is also introduced. Finally, the proposed integrated RF transmitter is described. In Section 3, simulation experiments of the proposed integrated RF transmitter using Cadence IC design tools are conducted, and the corresponding simulation results demonstrate its superior performance and functionality. Additionally, the parasitic analysis and interference effects are also introduced. Section 4 concludes this paper. Additionally, the full names of frequently used abbreviations in this paper are listed in Table 1.

Table 1. List of abbreviations

Abbreviation	Full Name
CMOS	Complementary metal-oxide-semiconductor
WSN	Wireless sensor network
VCO	Voltage-controlled oscillator
IIP3	Input-referred third-order intercept point
RF	Radio frequency
IF	Intermediate frequency
LO	Local oscillator
PA	Power amplifier
AC	Alternating current
DC	Direct current

2. Circuit Description

2.1. The voltage - controlled oscillator

Fig. 2 presents the schematic of the LC VCO utilized in the RF transmitter. The LC VCO consists of a frequency-selective LC tank and four transistors, comprising two NMOS and two PMOS devices. Fig. 3 depicts the AC equivalent circuit of the LC VCO. Here, the LC tank terminals are designated as A and B, with the ground identified as C. From the perspective of terminals A and B, transistors M_1, M_4 and M_2, M_3 constitute two independent single-port networks. It is assumed that all four transistors share identical characteristics, which is

$$g_{m1} = g_{m2} = g_{m3} = g_{m1} \tag{1}$$

where g_m is the transimpedance of the transistor.

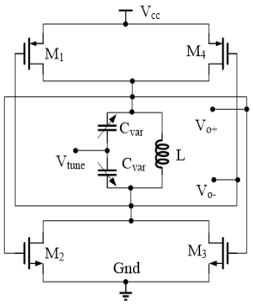

Fig. 2. The LC VCO.

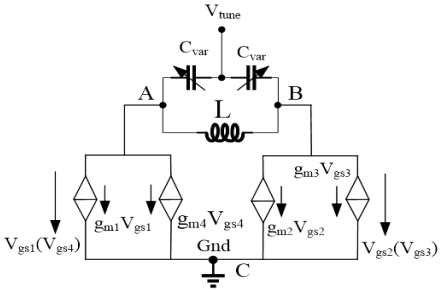

Fig. 3. The AC equivalent circuit of the LC VCO.

As evident from Fig. 2:

$$\begin{cases} V_{gs1} = V_{gs4} = V_{ds2} = V_{ds3} \\ V_{gs2} = V_{gs3} = V_{ds1} = V_{ds4} \end{cases} \tag{2}$$

Under steady-state operation of the VCO, the voltage amplitudes at terminals A and B become symmetrical and equal, leading to:

$$V_{ds1} = V_{ds4} = -V_{ds2} = -V_{ds3} \tag{3}$$

The AC equivalent conductance observed between terminals A and C can be formulated as:

$$G_{AM} = \frac{g_{m1}V_{gs1} + g_{m4}V_{gs4}}{V_{ds2}} \tag{4}$$

The input resistance observed between terminals A and B can be described as:

$$R_{in(AB)} = -(\frac{1}{2g_m} + \frac{1}{2g_m}) = -\frac{1}{g_m} \tag{5}$$

Building on the aforementioned analysis, Fig. 4 illustrates the simplified AC equivalent circuit of the LC oscillator.

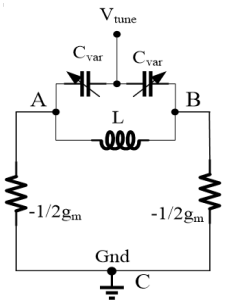

Fig. 4. The simplified AC equivalent circuit of the LC VCO.

The simplified equivalent circuit depicted in Fig. 4 [28] represents a conventional LC negative resistance oscillator [29, 30]. The overall negative resistance of the oscillator is approximately $-1/g_m$. When the negative resistance $-1/g_m$ matches the parasitic resistance of the LC parallel resonant tank $R_{in(AB)}$, it compensates for the energy losses in the tank, enabling the oscillator to sustain steady oscillation.

2.1.1. Phase noise analysis of the voltage - controlled oscillator

Phase noise is a crucial parameter in the performance of the LC VCO. It directly affects the spectral purity of the generated oscillation signals and consequently influences the overall performance of the RF transmitter. The phase noise of the LC VCO in this design is mainly determined by several factors. Firstly, the quality factor (Q) of the LC tank plays a significant role. A higher Q value indicates lower energy losses in the tank and thus results in lower phase noise. In this paper's design, efforts have been made to optimize the LC tank structure to achieve a relatively high Q value. The custom-configured LC tank, along with the careful selection of components, helps in reducing the resistive losses and parasitic effects, thereby contributing to the improvement of the Q value. Secondly, the noise generated by the transistors in the VCO also contributes to the phase noise. The stacked NMOS and PMOS transistor configuration is adopted not only to generate a robust negative resistance but also to minimize the noise contributions of the active devices. By carefully sizing the transistors and optimizing their biasing conditions, the flicker noise and thermal noise generated by the transistors can be effectively reduced. To quantitatively analyze the phase noise of the LC VCO, the well-known Leeson's equation is employed, i.e.: $L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_s}\left(1 + \frac{\omega_0^2}{2\Delta\omega^2 Q^2}\right)\left(1 + \frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right]$ where $L(\Delta\omega)$is the phase noise in

dBc/Hz at an offset frequency $\Delta\omega$ from the carrier frequency ω_0, F is the noise factor, k is the Boltzmann constant, T is the absolute temperature, P_s is the signal power at the output of the oscillator, and $\Delta\omega_{1/f^3}$ is the corner frequency of the $1/f^3$ noise.

Through theoretical calculations and simulation results based on the parameters of the designed LC VCO, the phase noise profile is obtained. The results show that at an offset frequency of 1 MHz from the carrier frequency of 1.15 GHz, the phase noise is approximately -110 dBc/Hz. This level of phase noise performance indicates that this LC VCO design can meet the requirements of the 2.4 GHz WSN applications in terms of signal purity and stability. Future research will continue to explore advanced techniques to further reduce the phase noise of the LC VCO. This may involve the use of new materials with lower loss characteristics for the LC tank, as well as the application of more sophisticated noise cancellation and suppression algorithms in the circuit design.

2.2. The sub-harmonic mixer

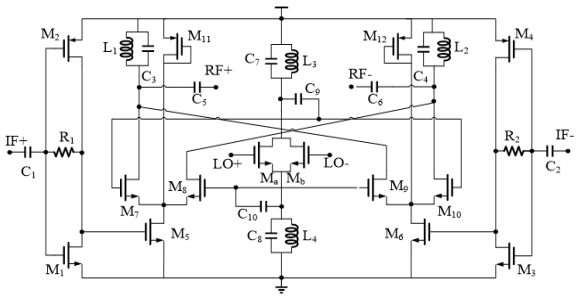

Fig. 5. The sub-harmonic mixer.

Fig. 5 illustrates the mixer utilized in the WSN transmitter. The transconductance input stage, composed of $M_1 - M_4$, R_1 and R_2 amplifies the received IF voltage signal and converts it into currents. The Gilbert switch core, formed by transistors $M_7 - M_{10}$, modulates the currents generated by the transconductance input stage. Transistors M_{11} and M_{12} implement the current-bleeding technique for the mixer, which enhances both the conversion gain and the IIP3 of the mixer. These two parallel LC tanks (L_1, C_3 and L_2, C_4) serve as the output loads for the mixer, functioning as band-pass filters. They resonate at 2.4 GHz, effectively rejecting unwanted interference signals. The LO frequency-doubling stage, composed of transistors M_a and M_b, is driven by the LO power supplied by the LC VCO. Since the frequency-doubling stage generates not only the $2f_{LO}$ frequency, but also all even harmonic frequencies ($4f_{LO}, 6f_{LO}, 8f_{LO}, \ldots\ldots$ nf_{LO}) in the output, two additional parallel LC tanks (L_3, C_7 and L_4, C_8) resonate at $2f_{LO}$, effectively rejecting the remaining unwanted even harmonic frequencies.

2.3. The proposed integrated radio frequency transmitter

The proposed integrated RF transmitter is shown in Fig. 6 [31], and it consists of a LC VCO and a sub-harmonic mixer presented in Fig. 2 and Fig. 5.

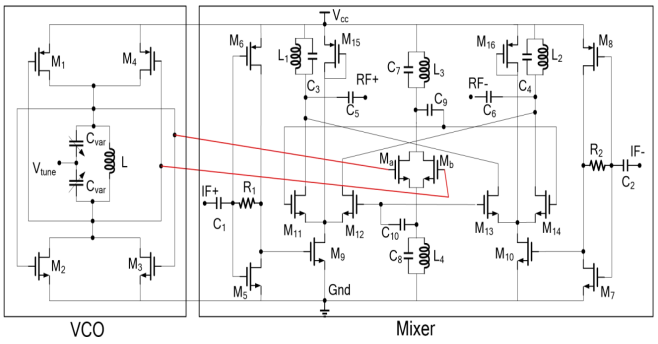

Fig. 6. The proposed integrated RF transmitter.

On the left side of the integrated RF transmitter, the LC VCO generates two sinusoidal waves with a 180° phase difference, supplying the necessary LO signals for the mixer. The two LO signals generated by the VCO are fed into the frequency multiplier, composed of transistors M_a and M_b. The frequency multiplier doubles the LO frequency, with the resulting frequency used as the actual LO signal for the mixer. The frequency of the LC VCO is set at 1.15 GHz, and through the frequency multiplier (M_a and M_b), the actual LO signal for the mixer becomes 2.3 GHz, effectively halving the required VCO frequency. Additionally, as shown in Fig. 6, the proposed integrated RF transmitter employs two stacked transistors in the DC path, including the load stage, with the mixer operating at a supply voltage of just 1 V.

3. Results and Discussion

3.1. Simulation results of the proposed integrated radio frequency transmitter

The design and simulation of the integrated RF transmitter are conducted using the advanced GlobalFoundries 0.18 μm RF CMOS process, which is widely recognized for its effectiveness in RF circuit design. The mixer is designed to operate with a low supply voltage of 1V, achieving an exceptionally low power consumption of only 2.55 mW, which underscores the energy-efficient characteristics of the transmitter. The simulation results, which are generated using the advanced Cadence IC design tools 5141 under the Linux environment, are presented in Fig. 7 - Fig. 10, demonstrating the performance and functionality of the integrated RF transmitter.

Fig. 7 illustrates the simulated output waveforms of the VCO. As depicted in Fig. 7, the LC VCO generates two sinusoidal signals that exhibit a precise 180° phase difference, which is critical for generating the LO signals required by the mixer [32]. The LC VCO operates at a frequency of 1.15 GHz, producing two sinusoidal signals with a peak amplitude of 980 mV, which are used as the LO signals for the integrated RF transmitter.

Fig. 8 shows the transient analysis of the proposed RF transmitter, providing a dynamic view of the transmitter's performance over time [33]. Here, the input IF signal is chosen to be 100 MHz, with an input power level of 20 dBm, representing typical signal characteristics encountered in WSN applications. As depicted in Fig. 8, the output RF signal affects the performance of

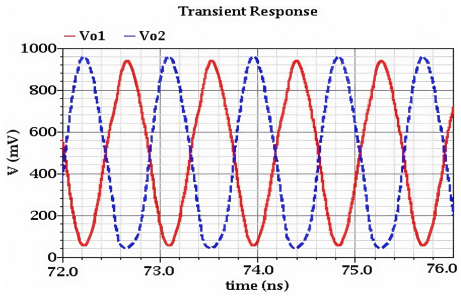

Fig. 7. The simulated outputs of the VCO.

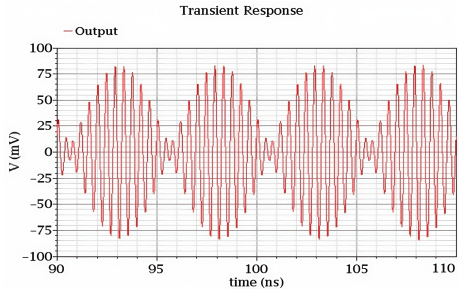

Fig. 8. The transient analysis of the proposed integrated RF transmitter.

the transmitter in terms of signal amplification and processing, showing the capability to handle the input IF signal effectively.

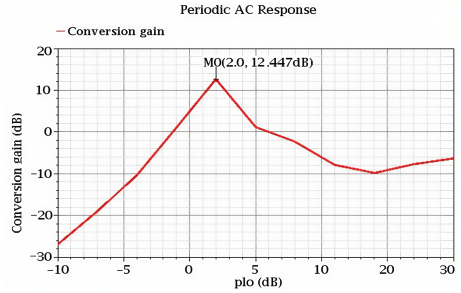

Fig. 9. Conversion gain of the integrated RF transmitter.

Fig. 9 illustrates the conversion gain characteristics of the integrated RF transmitter. Simulation results demonstrate that the proposed RF transmitter achieves a peak conversion gain of 12.447 dB, highlighting its exceptional signal amplification capability. Fig. 10 presents the power performance of the integrated RF transmitter, obtained through a two-tone harmonic simulation using input signals with a frequency separation of 1 MHz [34]. As depicted in Figure 10, the IIP3 of the integrated RF transmitter is approximately 3.19 dBm, which indicates its strong linearity performance.

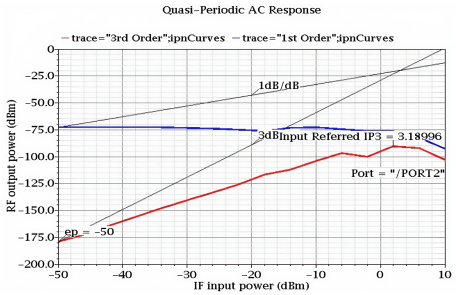

Fig. 10. The power performance of the integrated RF transmitter.

3.2. Performance comparison with related work

In order to fairly evaluate the performance of the proposed integrated RF transmitter, Table 2 compares the conversion gain and IIP3 of the proposed RF transmitter with related work in different papers. In terms of conversion gain, the proposed integrated RF transmitter reaches 12.447 dB. The conversion gain of Ref. [35] is 8.5 dB, which is lower than that of this paper. The conversion gains of [36], [37] and [38] are 12.7 dB, 13.6 dB, and 13.74 dB respectively, and they are slightly higher than that of this paper. Regarding IIP3, this paper has a value of 3.19 dBm, indicating relatively good linearity performance. Ref. [36] reaches 14.5 dBm, showing strong anti - nonlinear distortion performance. However, the IIP3 values of [36], [37] and [38] are - 6 dBm, - 4.46 dBm and - 3.5 dBm respectively, all of which are negative and significantly lower than that of this paper, meaning these designs are more prone to intermodulation distortion when dealing with multi-frequency signals and have relatively poor linearity.

Table 2. Performance summary and comparison

Reference	Frequency (GHz)	Conversion gain	IIP3
This paper	2.4	12.447	3.19
[35]	2	8.5	14.5
[36]	2.4	12.7	-6
[37]	2.4	13.6	-4.46
[38]	2.4	13.74	-3.5

In summary, this paper achieves a good balance between conversion gain and IIP3 linearity. Different studies have their own advantages and disadvantages. In the design of RF transmitters, it is necessary to balance these aspects according to specific application scenarios, which involves circuit topology, device parameter optimization, and is also closely related to factors such as power consumption and cost. The results of this paper provide valuable references for subsequent design optimizations, emphasizing that when pursuing high conversion gain, key performance indicators such as linearity cannot be ignored.

3.3. Discussion

There are two important factors should be considered in designing of RF transmitter. One is the impact of LC Tank's parasitic on VCO, and the other is the Impact of layout parasitic on VCO and mixer. The parasitic capacitances and resistances in the LC tank can affect the

resonant frequency and quality factor of the tank, and they may lead to a shift in the resonant frequency of the LC VCO. Generally, the parasitics of the LC tank can be effectively reduced by means of component selection, shielding measures and various compensation technology. Additionally, layout parasitic inductances due to the physical layout of the integrated circuit can cause additional phase shift and attenuation of the signal, especially at higher frequencies. In order to reduce the layout parasitic inductances, one may optimize the circuit layout, shorten the critical high-frequency signal path, and reduce parallel lines to avoid parasitic capacitance coupling.

4. Conclusions

This paper presented the design and simulation of a low-voltage, low-power integrated RF transmitter tailored for 2.4 GHz WSN applications, with a focus on optimizing both energy efficiency and compactness for long-term, autonomous operation in distributed environments. The integrated RF transmitter described in this paper is rigorously designed and simulated using GlobalFoundries' 0.18 μm RF CMOS process technology, with Cadence IC Design Tools 5141 utilized for detailed simulations and performance evaluation, ensuring that the design meets stringent WSN requirements. Simulation results indicate that the proposed RF transmitter achieves a conversion gain of approximately 10.5 dB, demonstrating its capability to effectively amplify the input signal for WSN applications while maintaining a compact design. Furthermore, the power consumption of the transmitter is exceptionally low, maintaining a value of just 2.55mW under a 1V supply voltage. This performance highlights the transmitter's suitability for low-power wireless sensor networks, where energy efficiency is paramount. In addition, the mixer demonstrates an IIP3 of 3.19 dBm, indicating its effectiveness in handling third-order nonlinearities. This characteristic ensures that the proposed RF transmitter performs well even in the presence of strong interfering signals, which is a common requirement of WSNs. In future work, using more advanced integrated circuit technology to design RF transmitters with better performance is one of the research directions. Moreover, the fabrication of the integrated RF transmitter and applied it in the real WSN is another research direction.

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