

A Novel Current-Mode Capacitor Multiplier for Improved Noise Filter

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Abstract. This paper presents a novel current-mode capacitor multiplier that offers a superior alternative to existing solutions. By simply adding a resistor, the proposed circuit achieves multiplied equivalent capacitance, outperforming state-of-the-art implementations. Simulation results demonstrate the circuit's effectiveness in a noise filtering application for a voltage reference, requiring only a 100pF integrated capacitor and 2μA quiescent current to achieve a 16Hz low cut-off frequency. Compared to traditional solutions, the proposed multiplier reduces the required capacitor size from 10nF to 100pF. The new design excels in both power supply rejection ratio and noise performance, making it an attractive solution for low-power, high-precision applications.

Key-words: Capacitor multiplier; low-pass filter; noise; low quiescent; voltage reference.

1. Introduction

In recent years, the development of modern electronic systems has been increasingly directed toward achieving better functionality, reduced size, and enhanced energy efficiency. In this context, the integration and miniaturization of more and more analog circuits have become a critical area of focus. Analog ICs form the foundation of electronic systems that interact with

the physical world, enabling fundamental operations such as power regulation, signal sensing, amplification, filtering, and signal conversion. The effective functionality of these circuits is intrinsically reliant on essential building blocks, including transistors, resistors, and capacitors – each fulfilling distinct yet complementary roles within the system’s architecture. Transistors and resistors are indispensable for functions such as amplification, active switching, and current regulation. Equally important is the capacitor integration. These components perform numerous key functions, including noise filtering, charge storage, frequency compensation in control loops, timing operations, frequency stabilization for oscillators, and AC coupling. Collectively, these elements underpin the critical importance of capacitors for optimizing the performance and efficiency of analog ICs within modern electronic systems. Consequently, analog integrated systems often require high-value capacitors characterized by high accuracy and linearity that occupy small silicon area. Although, this is difficult to achieve, given the fact that two polysilicon layers or to metal layers available in modern fabrication processes typically result in relatively small capacitive values. Even if the MOS capacitor is taken in consideration which usually is more area efficient, the large capacitor values are hard to be achieved.

These considerations have motivated designers to develop various architectures including active devices for capacitance multiplication. Some schemes offer a very high multiplication factor, although they have poor accuracy [1–4]. Others offer very high accuracy at the expense of increased silicon area and power consumption [5, 6].

This work extends the CAS paper with explicit calculations and trade-off analysis of state-of-the-art capacitor multipliers and the proposed design, applied as a noise filter for a Kujik bandgap voltage reference whose full design is included. It consolidates known voltage-reference noise filters with clear pros/cons, and uses a dedicated testbench to compare the proposed multiplier against an ideal filter and current SOTA solutions. Simulated results include PSRR for the unfiltered reference and for three specific filtering variants, plus noise density and transient noise simulations to demonstrate performance gains. The paper also adds updated, noise-focused references aligned with the ROMJIST scope.

The paper is organized in 5 sections. After the introduction, in Section 2 the state-of-the-art capacitor multipliers are presented followed by the detailed description of the proposed solution (Section 3). The main and most consistent part of the paper is presented in Section 4 where the use case is described together with the testbenches and simulation results. Lastly, the paper is concluded by Section 5.

2. State-of-the-art of Capacitor Multipliers

A capacitor multiplier is a circuit that emulates the behavior of a large physical capacitor by utilizing active components, such as transistors, and circuit architectures that scale the effective capacitance. This approach significantly enhances area efficiency on-chip while achieving the desired capacitive characteristics necessary for certain applications.

Based on their working principle, capacitor multipliers can be categorized into two main types: voltage-mode and current-mode multipliers.

2.1. Voltage mode capacitor multipliers

The voltage-mode multipliers rely on the well-known Miller effect, leveraging the extremely high gain of the amplifying stage to achieve a large multiplication factor (Fig. 1). The resulting

equivalent capacitor in this configuration is often referred to as a Miller capacitor [7].

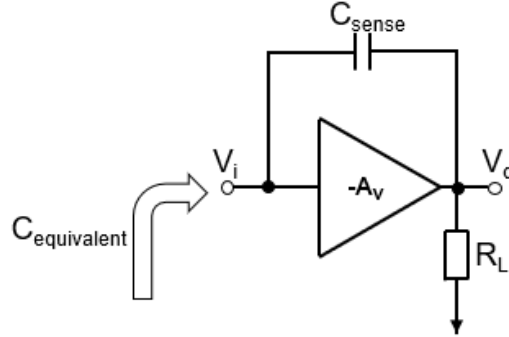


Fig. 1. Example of a generic voltage mode capacitor multiplier.

Considering the circuit in Fig. 1, the equivalent capacitor can be expressed:

$$C_{equivalent} = (1 + |A_V|) C_{sense} \tag{1}$$

Relation (1) shows that the multiplication factor depends on the amplifier gain (A_V) which in practice depends on parameters like transconductance gain (g_m), drain-source resistance (r_{ds}) of a transistor, resistors values etc. Being affected by fabrication process, temperature, and voltage across terminals, the multiplier accuracy is significantly compromised. Additionally, the dynamic range is considerably limited, due to the fact that a very small amplitude may cause the saturation of the amplifying stage output, introducing undesired distortion or malfunction [4, 7].

2.2. Current mode capacitor multipliers

In this paper, similar with [1–3, 5, 6], the proposed circuit is based on the second type structure, the current-mode capacitance multipliers. Fig. 2 shows the concept of operation, wherein the current sensed by a capacitor (C_{sense}) flows through the diode connected transistor M1 and multiplied by factor k through the current mirror M1–M2. As a result, the current through M2 becomes $k \cdot i_{sense}$, resulting in a total equivalent current $(1 + k) \cdot i_{sense}$.

Therefore, the equivalent capacitance becomes:

$$C_{equivalent} = \left(1 + \frac{g_{m2}}{g_{m1}}\right) C_{sense} = (1 + k) C_{sense} \tag{2}$$

In the current-mode capacitor multiplier illustrated in Fig. 2, the accuracy of the multiplication factor is significantly improved. Rather than relying on absolute parameter values, it is solely determined by the ratio of the parameters (2). Moreover, the input voltage swing is highly increased leading to an extended domain limited only by the saturation voltages of M2 and the bias current $k \cdot I_B$, respectively.

Beside the multiplication factor, the equivalent series resistance (ESR) is another critical parameter for capacitance multipliers. Assuming the transistors parasitic capacitance is negligible compared to the sense capacitor and drain to source conductance g_{ds2} is much lower than its transconductance g_{m2} .

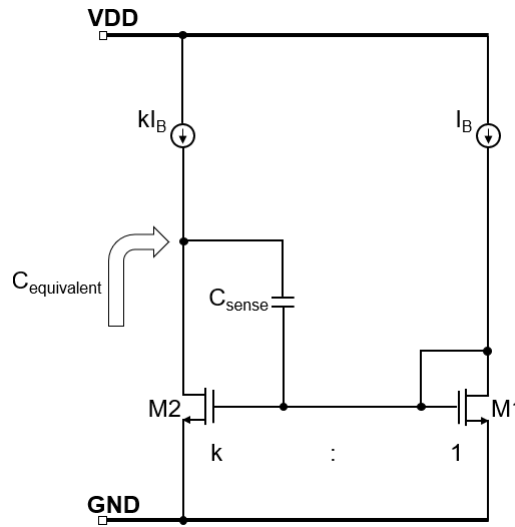


Fig. 2. Example of a current mode capacitor multiplier [8].

The ESR can be determined by calculating the equivalent impedance of the capacitor:

$$Z_C \cong \frac{1 + j\omega \frac{C_{sense}}{g_{m1}}}{j\omega(1+k)C_{sense}} \quad (3)$$

Based on (3), as the frequency increases, the capacitor starts to behave like a resistor and the ESR becomes $\frac{1}{(1+k)g_{m1}}$. Thus, its value can be adjusted by modifying the transconductance of M1 while maintaining the same mirroring factor.

For the circuit in Fig. 2, large k values significantly increase the current consumption which is proportional to I_B , while also requiring greater silicon area for M1–M2. Moreover, the accuracy of the current mirror degrades at higher mirroring ratios, despite the application of proper layout techniques [8].

There are various methods available to address the aforementioned disadvantages [1–3, 5, 6]. However, these solutions are often more sophisticated and require multiple additional components, such as operational transconductance amplifiers (OTAs), current mirrors, buffers, or another circuitry. For this reason, a novel capacitor multiplier is proposed.

3. Proposed Capacitance Multiplier Circuit

The preceding arguments underscore the necessity for an innovative and straightforward method to amplify the effect of a capacitor, as demonstrated in Fig. 3. The novelty of this approach lies in the introduction of a resistor R_m placed between the gates of M2 and M1. Under DC operation, the resistor has no influence due to zero gate current. However, in the AC regime, the mirroring ratio is effectively enhanced from k to $k(1 + g_{m1}R_m)$, significantly increasing its impact [8, 9].

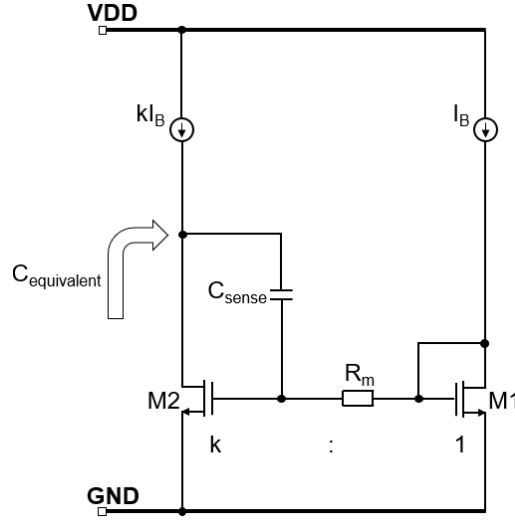


Fig. 3. Proposed capacitor multiplier [8].

Consequently, the new equivalent capacitance can be expressed as follows:

$$C_{equivalent} = [1 + k(1 + g_{m1}R_m)] C_{sense} \quad (4)$$

Equation (4) demonstrates that substantial multiplication factors can be achieved through the appropriate sizing of resistor R_m , without compromising the DC functionality, such as mismatch or current consumption (setting $k = 1$). However, a hybrid approach can be employed, leveraging both the resistor R_m and an acceptable k ratio to optimize the overall performance.

Similar to the state-of-the-art current mode multiplier, the equivalent series resistance (ESR) of the resulting capacitor can be determined by formulating the input impedance equation:

$$Z_C \cong \frac{1 + j\omega \left(R_m + \frac{1}{g_{m1}} \right) C_{sense}}{j\omega [1 + k(1 + g_{m1}R_m)] C_{sense}} \quad (5)$$

Equation (5) reveals that when R_m is significantly larger than $1/g_{m1}$, the ESR can be approximated by $1/g_{m2}$. This implies that, at high frequencies, C_{sense} effectively shorts the drain of M2 to its gate, causing it to behave similarly to a diode-connected configuration.

Further analyzing the circuit, it becomes evident that the enhanced gain factor presented in (4) is sensitive to process and temperature variations due to the $g_{m1}R_m$ product. To overcome this limitation, a more robust structure has been presented in CAS conference in 2025, wherein the resistor R_m is replaced with a transistor operating in the linear region. Using the same type of transistor as M1, M2, the multiplier variations caused by external factors are minimized while maintaining the initial functionality [8, 9]. Nevertheless, the improved structure is beyond the scope of this paper, as the primary focus is not on the accuracy of the obtained capacitor. Instead, the emphasis is placed on the multiplication factor and the noise characteristics, which are the dominant considerations in this study.

4. Noise Filter for a Kujik Bandgap Voltage Reference

Noise filtering is a crucial aspect of precision circuit design, particularly when it comes to Bandgap voltage references. The output noise of these references can be mitigated using various techniques, each with its own advantages and trade-offs.

Some common methods for filtering output noise include passive filtering, which utilizes components such as resistors, capacitors, and inductors to attenuate the noise [2, 3, 6]. Another approach is chopping, which involves modulating the signal at a high frequency to reduce noise and increase precision [10]. Increasing the current consumption of the circuit is also a technique used to reduce noise, as it can help to improve the signal-to-noise ratio. However, this approach often comes at the cost of increased power consumption, which can be a significant concern in power-sensitive applications. The choice of technique depends on the specific requirements of the application, including the desired level of precision, power consumption, and area efficiency.

The selection of a passive filtering method can be a challenging task, particularly when aiming to achieve low cut-off frequencies in the Hz range. This is due to the large capacitor values required, which can be difficult to implement on-chip.

One possible solution is to use an external capacitor, but this approach comes with several drawbacks, including increased Bill of Materials (BOM) cost, the need for an additional pin on the chip, potential leakage at the pin, and the requirement for a dedicated start-up circuit to pre-charge the capacitor. These disadvantages make the use of an external capacitor less attractive.

In contrast, using an internal capacitor can be a more appealing option, as it eliminates the need for an external component and reduces the overall system cost. However, the main limiting factor for on-chip capacitors is the silicon area required, which can be a significant constraint.

To overcome this limitation, capacitor multipliers can be considered as a viable solution, using a small physical capacitor, thereby reducing the silicon area required. However, the design of these circuits requires careful consideration of factors such as noise, linearity, and power consumption.

4.1. Voltage reference design and testbench generation

The primary objective of this paper is to develop an area-efficient low-pass noise filter tailored for a generic voltage reference. The selected architecture for this purpose is a Kujik voltage reference, as illustrated in Fig. 4.

The circuit depicted in Figure 4 has been implemented using Infineon's proprietary 130nm CMOS technology. A key design constraint is to ensure that the total quiescent current, including the filter, does not exceed 10 μA . The Bandgap core is composed of a 1:24 vertical PNP structure and an error amplifier, which regulates the output voltage of the circuit. The resistors were carefully sized to achieve a first-order temperature-compensated voltage reference while maintaining a typical current consumption below 6 μA , considering also a start-up circuit not shown in the schematic. With optimized circuit design, the output voltage is approximately 1.217V at nominal temperature.

The stringent requirement for low quiescent inherently affects the noise performance of the voltage reference. As a result, the implemented filter is designed to fulfill two critical functions: first, to attenuate the low frequency intrinsic noise generated within the reference circuit (in the 10Hz – 100kHz bandwidth); and second, to suppress noise coupled from the VDD supply line, ensuring improved overall stability and performance.

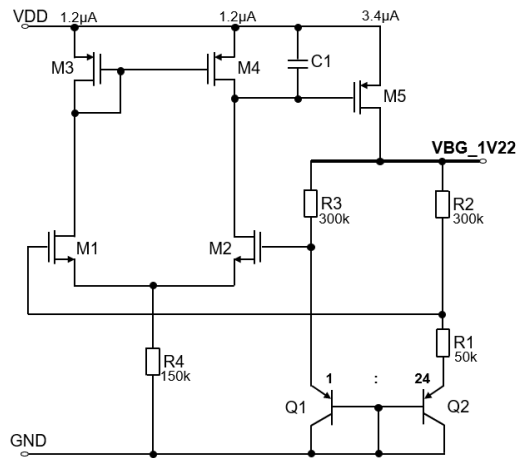


Fig. 4. Kujik Bandgap reference.

To meet the resulted requirements, the proposed capacitor was integrated into a low-pass filter in conjunction with a $1\text{M}\Omega$ resistor. This configuration results in a cut-off frequency of approximately 16 Hz. To accurately assess the performance of the filter, a dedicated testbench was developed, as shown in Fig. 5. The testbench incorporates three filter variants for comparative analysis:

- a filter utilizing a $1\text{M}\Omega$ polysilicon resistor and a placed 10nF capacitor (Fig. 5a),
- a filter employing the same resistor and a state-of-the-art capacitor multiplier (Fig. 5b),
- a filter using the proposed circuit in combination with the same $1\text{M}\Omega$ resistor (Fig. 5c).

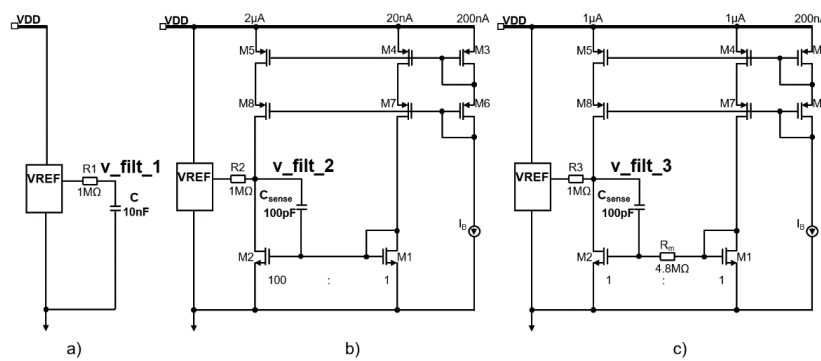


Fig. 5. Three filter variants: a) using a real capacitor b) using SOTA c) using proposal.

Both capacitor multiplier circuits utilize a 100pF sense capacitor. To achieve a $100\times$ amplification factor, the SOTA multiplier employs a 1:100 current mirror, whereas the proposed solution incorporates a 1:1 current mirror in combination with a $4.8\text{M}\Omega$ resistor. To maintain equal total current consumption, both capacitor multipliers operate with the same 200nA reference current,

but differ in the bias current distribution within their branches. Specifically, in the configuration shown in Fig. 5b, the SOTA multiplier has a current of 20nA flowing through M1 and 2 μ A through M2 (reflecting the 1:100 ratio). In contrast, in the proposed solution depicted in Fig. 5c, M1 and M2 both operate with an equal current of 1 μ A. The next analysis will proceed with a fixed supply voltage of 2.5V.

4.2. Transfer function analysis

The initial analysis conducted was an AC simulation to examine the frequency response of the three filters. The results, presented in Fig. 6, highlight the attenuation performance of each filter across the frequency range of interest, spanning from 10 Hz to 100 kHz.

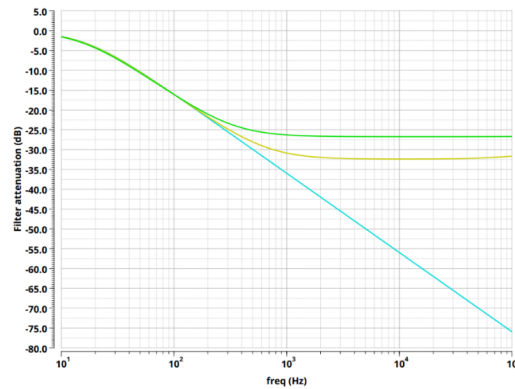


Fig. 6. Filters attenuation vs frequency.

Simulation results indicate that all three filters exhibit a similar cut-off frequency of approximately 16 Hz and presents comparable behavior up to 200Hz. Beyond this frequency, the attenuation of the filters employing the multiplied capacitors begins to saturate when compared to the ideal characteristics (Fig. 6, blue curve). Nevertheless, the proposed circuit (green curve) achieves an attenuation of approximately 26dB, while the SOTA approach (yellow curve) reaches 32dB. These values correspond to an approximate attenuation of 20 and 40 times, respectively, both of which are well within acceptable limits for the targeted objective. The 6dB difference between the proposed filter and the SOTA implementation is attributed to the difference in equivalent series resistance (ESR). Although the transistors in the lower current mirror of both designs were sized to achieve the same g_m/I_D ratio, the reduced bias current of 1 μ A in the proposed circuit, compared to 2 μ A in the SOTA design, results in a lower transconductance g_m and, consequently, a higher ESR value. By comparing the attenuation values and considering the 1M Ω filters resistor, it is deduced that the ESR of the SOTA design is approximately 25k Ω , whereas the ESR of the proposed design is around 50k Ω .

4.3. Power supply rejection

The second analysis evaluates the small-signal power supply rejection ratio (PSRR). The result, presented in Fig. 7, compare the performance of the three filter configurations. The red curve represents the PSRR of the reference generator without any filtering, while the blue one

corresponds to the output of the first filter variant. The yellow and green curves correspond to the PSRR of the SOTA and the proposed cap-multiplier, respectively. Although the SOTA multiplier exhibits higher attenuation in Fig. 6, the proposed solution achieves better overall PSRR performance. This improvement can be attributed to its reduced sensitivity to noise coupled through PMOS current mirrors, which arises from the different branches biasing.

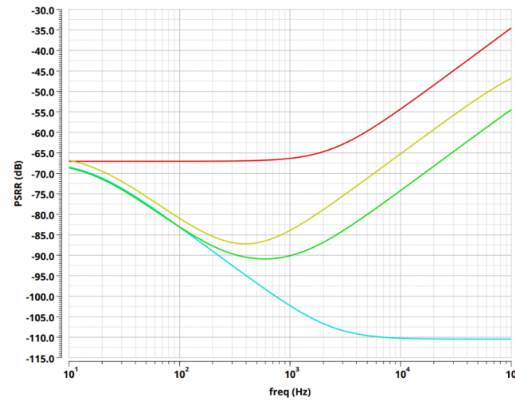


Fig. 7. PSRR vs frequency.

The results demonstrate that the inclusion of filters significantly enhances the PSRR, with similar improvements observed across all configurations up to 200 Hz, consistent with the behavior noted in Fig. 6. Notably, they provide 14dB additional rejection at 100Hz, approximately 20dB at 1kHz, and more than 10dB extra rejection for frequencies above 10kHz.

4.4. Noise analysis

The final analysis focuses on noise. Figure 8 illustrates the simulated noise spectral density across the defined frequency range, along with the integrated noise values (RMS noise) in the 10Hz–100kHz range. The color coding follows the same scheme used in previous graphs. The Bandgap generator exhibits an RMS noise of 134.9 μ V (red curve) without any filtering. When the first filter implementation (an ideal filter, represented in blue) is applied, noise is reduced across the entire frequency spectrum, resulting in an approximately seven times decrease in RMS noise to 19.2 μ V.

Despite having the same cut-off frequencies and similar behavior in the tens to hundreds of Hz range, filters utilizing the capacitor multiplier technique display different noise density behavior. This discrepancy is explained by the inherent noise characteristics of the structures. Notably, the SOTA filter is highly inefficient in the low-frequency range (yellow curve), yielding an RMS noise value (160.6 μ V) even higher than that of the unfiltered voltage reference. While not flawless, the proposed capacitor multiplier-based filter introduces minimal additional noise (notably between 10–20Hz) and manages to attenuate the integrated noise by more than 3.6 times, reducing it to 37.2 μ V.

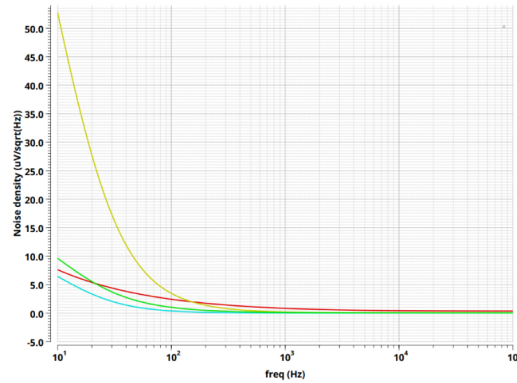


Fig. 8. Noise spectral density.

The disparity in noise performance between the two multipliers can be attributed to the fundamental differences in their multiplication architectures. The diode-connected transistor M1 is the primary root-cause of noise in both configurations, with its biasing current being a critical determinant of noise magnitude [11]. Specifically, the first case operates with a relatively low bias current of 20nA, whereas the proposed circuit employs a significantly higher bias current of 1 μ A, thereby mitigating noise contributions. Moreover, the state-of-the-art circuit exacerbates noise through a 100-fold amplification of M1's noise, whereas the proposed structure exhibits a more favorable 1:1 ratio and incorporates also filtering via the 4.8 M Ω resistor and the Miller capacitor seen in gate of M2, thus yielding improved noise performance [11, 12].

For a better understanding of the noise behavior, a transient noise simulation was conducted utilizing the noise models associated with the technology employed for the design. The results of this simulation are illustrated in Fig. 9, which depicts the output waveforms of the three filters, as well as the original voltage reference without filtering (represented in red).

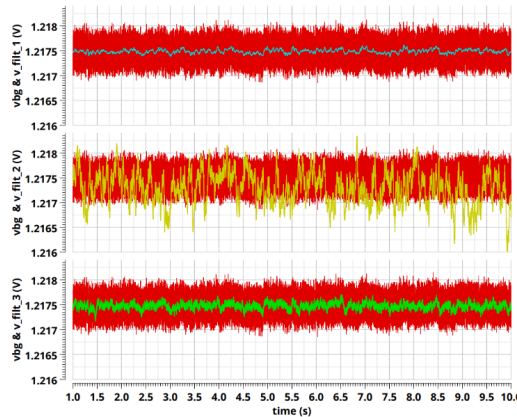


Fig. 9. Transient noise.

The transient noise in Fig. 9 demonstrate effective attenuation of high-frequency noise by the first filter, which features a 10nF placed capacitor (blue waveform). However, the state-of-the-art filter exhibits higher low-frequency amplitudes compared to the original voltage reference (yel-

low waveform), despite its ability to filter out high-frequency spikes. In contrast, the proposed circuit (green) displays improved overall performance, successfully rejecting high-frequency and low-frequency noise. This is consistent with the calculated root mean square noise value, indicating a more effective noise reduction circuit.

4.5. Performance summary

The results of the previous analysis and simulation studies have been compiled in a comparative format, as shown in Table 1, to evaluate the performance of different filter implementations.

Table 1. Performance comparison

	BG + Filter 1	BG + Filter 2	BG + Filter 3
Filter capacitor	10nF	100pF	100pF
Multiplication factor	–	100	100
PSRR @ 1kHz [dB]	102	84	90
RMS Noise 10Hz – 100kHz [μ V]	19.2	160.6	37.2
Current consumption [μ A]	6	8.2	8.2
Area	100A	1.1A	1.1A

Firstly, it is evident that both capacitor multipliers achieve a significant reduction in filter capacitor size, from 10nF to 100pF. The proposed filter exhibits better PSRR compared to SOTA, being much closer to the ideal characteristics of the first filter. Furthermore, the RMS noise indicates that the second variant exhibits a substantially higher noise level of 160.6 μ V, surpassing the noise levels of the first filter variant (19.2 μ V) and the proposed circuit (37.2 μ V). Notably, the noise level of SOTA even exceeds 134.9 μ V of the original voltage reference, rendering it unsuitable for low-noise applications.

Both capacitance multiplier circuits have a relatively modest impact into the total quiescent current, adding only 2.2 μ A to the 6 μ A of original of the voltage reference circuit.

Finally, the area is reduced by a factor of 90, from 100 times the reference area to only 1.1 times when using any of the capacitor multipliers.

5. Conclusions

In this paper a novel current-mode capacitor multiplier was proposed and analyzed. It offers a superior alternative to the state of the art, obtaining the multiplied equivalent capacitance in a simple manner (by only adding a resistor). Over the course of the article, the proposed circuit was compared with other two implementations (one for benchmarking, the other being the state of the art) by simulating a noise filtering application of a voltage reference. This experiment shows that in order to obtain a low cut-off frequency (16Hz), it requires only a 100pF integrated capacitor and 2 μ A quiescent current, instead of 10nF real capacitor. The proposed solution stands out from the state of the art for both PSRR and noise performance.

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